REFERENCE DESIGN AVAILABLE

MAX2552

Band III, IV, IX, and X WCDMA Femtocell Transceiver with GSM Monitoring

General Description

The MAX2552 is a complete single-chip RF-to-bits and bits-to-RF radio transceiver. This device is in compliance with the 3GPP TS25.104 femtocell standard for Band III, IV, IX, and X. It is equipped with multiple receive inputs and transmit outputs for low band, high band, and macro-cell monitoring (Table 1).

This fully integrated transceiver facilitates compact radio designs for dongle and stand-alone femtocell products by minimizing external component count. Maxim's MAX-PHY serial interface is used to drastically reduce IC pin count, while worldwide field-proven architecture accelerates time to product deployment.

The device features unparalleled receive blocker performance and the industry's lowest noise figure for higher data rates and range. Low-power operational modes are available to minimize power consumption. The transmitter is designed to deliver EVM far exceeding the standard requirement at 0dBm.

The MAX2552/MAX2553 is a family of pin-compatible transceivers that cover all major WCDMA and cdma2000® bands. All parts are controlled by a 4-wire interface.

The MAX2552 is packaged in a compact 7mm x 7mm TQFN and specified over the -40°C to +85°C extended temperature range. A complete radio reference design is available to facilitate custom designs.

Applications

WCDMA Band III, IV, IX, and X Femtocells

***Ordering Information* and *Simplified Block Diagram* appear at end of data sheet.**

*For related parts and recommended products to use with this part, refer to **www.maximintegrated.com/MAX2552.related**.*

Features

- **Single-Chip Femtocell Radio Transceiver**
- **WCDMA/HSPA+ Band III, IV, IX, and X Operation**
- **TS25.104 Standard Compliant**
- **Multiple LNA Inputs for WCDMA, PCS, and GSM Macrocell Monitoring (Bands II, III, IV, V, IX, and X)**
- **High Level of Integration**
  - **On-Chip Fractional-N Frequency Synthesizers for LO Generation**
  - **No Tx SAW Filters Required**
  - **Integrated PA Drivers for Lower-Cost Power Amplifier Designs**
  - **12-Bit AFC DAC to Control TCXO**
  - **On-Chip Temperature Sensor**
  - **Three General-Purpose Outputs**
  - **Reference Clock with Selectable CMOS and Low Swing Output**
  - **PLL Lock-Detect Output Through GPO3**
- **Optimized Receiver Performance**
  - **Exceptional Receive Sensitivity**
  - **High Dynamic Range Sigma-Delta ADCs Allow Simple AGC Implementation with Switched Gain States**
- **Optimized Transmitter Performance**
  - **Factory Calibrated for Gain, Carrier Leakage, and Sideband Suppression**
  - **10-Bit Gain-Control Resolution for Better Power Accuracy**
  - **60dB Gain-Control Range**
- **Loopback Operating Mode from Tx Baseband Input to Rx Baseband Output**
- **MAX-PHY Serial Digital Interface**
- **SPI Read/Write Functionality**
- **Operation Controlled by 4-Wire Serial Interface**
- **Low-Cost, 7mm x 7mm TQFN Package**

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-6678; Rev 0; 4/13

MAX2552

Band III, IV, IX, and X WCDMA Femtocell Transceiver with GSM Monitoring

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ABSOLUTE MAXIMUM RATINGS

$V_{CC\_}$ to GND_ ..... -0.3V to +3.9V
RXIN_, MIXIN_, LNAOUT_ to GND_ ..... -0.3V to +1.2V
All Pins Except $V_{CC\_}$ to GND_ ..... -0.3V to ($V_{CC\_}$ + 0.3V)
AC Input Signals ..... 1.0V Peak
Digital Input Current ..... ±10mA
Maximum VSWR Without Damage 8:1

Continuous Power Dissipation (T_A = +70°C)
TQFN Multilayer Board (derate 40mW/°C above +70°C) ... 3.2W
Junction Temperature ..... +150°C
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 25°C/W

Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC ELECTRICAL CHARACTERISTICS

($V_{CC\_}$ = 3.0V to 3.6V, 50Ω system, f_{REFIN} = 19.2MHz. T_A = -40 to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C, unless otherwise noted. Register settings as defined in tables following the specification tables.) (Note 2)

SPEC NO.	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC1	Supply Voltage	$V_{CC\_}$		3.0	3.3	3.6	V
DC19	Operating Supply Current WCDMA	$I_{CC\_}$	Full-duplex high band		300	419	mA
DC20			RXIN2 monitor		78	110	
DC21			RXIN4 monitor		70	100	
DC22			RXIN5 monitor		71	100	
DC23			Tx only		250	360	
DC24			Idle Rx		36		
DC25			Idle Tx		40		
DC3	Operating Supply Current AFC-Only Mode	$I_{CC\_}$	AFC DAC and SPI only		190	1000	µA
DC5	Operating Supply Current Reference Buffer Mode	$I_{CC\_}$	REFOUT = 500Ω ll 22pF, all else = off		6	7.5	mA
DC6	Operating Supply Current Sleep Mode	$I_{CC\_}$	All functions off		18	1000	µA
DC11	Digital Input Logic-High			1.3			V
DC12	Digital Input Logic-Low					0.4	V
DC13	Input Current for Digital Control Pins					10	lµAl
DC16	GPO Sink Current		V_{OUT} = 0.35V, DOUT_DRV = 01	1.0	1.8		mA
DC17	GPO Source Current		V_{OUT} = $V_{CC\_}$ - 0.3V, DOUT_DRV = 01	1.0	1.9		mA

AC ELECTRICAL CHARACTERISTICS

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band III, IV, IX, and X Duplexer Specifications

(Diplexer between antenna and duplexer loss: 0.3dB (applies to all Rx modes).)

Antenna—Uplink Port (Applies to Uplink WCDMA Rx Mode on RXIN1)

BAND (MHz)	Uplink 1710 to 1785	1 to 1660	1660 to 1710	1785 to 1825	1825 to 2200	2200 to 2500	2500 to 4500	4500 to 12750
ATTENUATION (dB)	Attenuation	Minimum Attenuation						
	2	32	12	12	37	27	12	7
Rx SAW FILTER RESPONSE								
BAND (MHz)	Out of band							
ATTENUATION (dB)	Required minimum attenuation relative to in-band							
	25							

Band III, IV, IX, and X Uplink WCDMA Rx Mode on RXIN1 (Full Duplex)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb4fu-0	Frequency Band	WCDMA FDD Band III uplink (lowest to highest channel center frequency)	1712.4		1782.4	MHz
		WCDMA FDD Band IV uplink (lowest to highest channel center frequency)	1712.4		1752.6	
		WCDMA FDD Band IX uplink (lowest to highest channel center frequency)	1752.4		1782.4	
		WCDMA FDD Band X uplink (lowest to highest channel center frequency)	1712.4		1767.6	
Wb4fu-1	Sensitivity 3GPP TS25.104 Section 7.2.1	Tx on at -27dBm, LNA gain mid-gain, PGA gain register set to 9, assumed SNDR > -17.5dB at sensitivity, using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-117	-107	dBm
Wb4fu-1a	Sensitivity with LNA in High-Gain Mode	Tx on at -27dBm, LNA gain high, PGA gain register set to 6, assumed SNDR > -17.5dB at sensitivity, using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-119	-107	dBm

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band III, IV, IX, and X Uplink WCDMA Rx Mode on RXIN1 (Full Duplex) (continued)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb4fu-3	High-Level EVM WCDMA	P_{IN} = -20dBm, LNA gain low, PGA gain register set to 1		3.8		%
Wb4fu-4	Sensitivity with Adjacent Channel Interference 3GPPP TS25.104 Section 7.4.1	Tx on -27dBm, LNA gain high, PGA gain register set to 3, assumed SNDR > -17.5dB at sensitivity, inferring signals at front-end input -28dBm, at 5MHz offset and -10MHz offset and modulated as in 3GPP, using UL reference measurement channel, (12.2kbps) as specified in A.2 3GPP 25.104, Production tested by measurement if SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-100		dBm
Wb4fu-5	Sensitivity with In-Band Blocking Interference 3GPPP TS25.104 Section 7.5.1	Tx on -27dBm, LNA gain high, PGA gain register set to 6, assumed SNDR > -17.5dB at sensitivity, inferring signals at front-end input -30dBm, at 10MHz offset and -10MHz offset and modulated as in 3GPPP, using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104, production tested by measurement if SNDR at output on CW input signal at -90dBm test only worst case in production, SNDR at MAX-PHY filter output established with FFT		-115	-101	dBm
Wb4fu-6	Sensitivity with Out-of-Band Blocking Interference 3GPP TS25.104 Section 7.5.1	Front-end assumed response as above, Tx on at -27dBm, LNA high gain, PGA gain register set to 6, assumed SNDR > -17.5dB at sensitivity, interfering signal at front-end input -15dBm CW, 1MHz to 1690MHz and 1805MHz to 12750MHz using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT (Note 3)		-116	-101	dBm

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band III, IV, IX, and X Uplink WCDMA Rx Mode on RXIN1 (Full Duplex) (continued)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb4fu-8	Sensitivity with Intermodulation Interference 3GPP TS25.104 Section 7.6.1	Tx on at -27dBm, LNA gain high, PGA gain register set to 6, assumed SNDR > -17.5dB at sensitivity; interfering signals at front-end input -38dBm, at 10MHz offset (CW) and 20MHz offset (modulated) as in 3GPP, using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT (Note 3)		-116	-101	dBm
Wb4fu-10	Spurious Emissions Out-of-Band 3GPP TS25.104 Section 7.7.1	30MHz to 1GHz, measured in 100kHz BW		-100	-60	dBm
		1GHz to 12.75GHz, measured in 1MHz BW, with the exception of frequencies between 12.5MHz below the first carrier frequency and 12.5MHz above the last carrier frequency used by the BS (Note 3)		-75	-50	
Wb4fu-11	Spurious Emissions in Receive Bands 3GPP TS25.104 Section 7.9.2	Front-end assumed response as above, 1710MHz to 1785MHz (Note 3)		-95	-80	dBm
Wb4fu-12	Conversion Gain High LNA Gain	LNA high gain, PGA gain register set to 6, tested on CW input signal at -90dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	23	31	36	dB
Wb4fu-13	Conversion Gain Mid LNA Gain	LNA mid gain, PGA gain register set to 9, tested on CW input signal at -90dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	23	31	36	dB
Wb4fu-14	Conversion Gain Low LNA Gain	LNA gain low, PGA gain register set to 1, tested on CW input signal at -20dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	-13	-6.5	-3	dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Antenna—Downlink Port (Applies to Downlink WCDMA Rx Mode on RXIN5)

BAND (MHz)	Downlink 2110 to 2170	1 to 2025	2025 to 2050	2050 to 2095	2185 to 2230	2230 to 2255	2255 to 12750
ATTENTUATION (dB)	Attenuation	Minimum Attenuation					
	2	15	10	0	0	10	15

Band IV and X Downlink WCDMA Rx Mode on RXIN5 (Monitor)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb4fd-0	Frequency Band		2112.4		2167.6	MHz
Wb4fd-1	Sensitivity 3GPP TS25.101 Section 7.3.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity, using UL reference measurement channel, (12.2kbps) as specified in C.3.1 3GPP 25.101, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-109	-101	dBm
Wb4fd-4	Sensitivity with Adjacent Channel Interference 3GPP TS25.101 Section 7.5.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity, interfering signals at front-end input -52dBm, at 5MHz offset and -5MHz offset and modulated as in 3GPP, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, production tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-103		dBm
Wb4fd-4a	Sensitivity with Adjacent Channel Interference 3GPP TS25.101 Section 7.5.1 CASE 2	LNA gain medium, PGA gain register set to 6, tested SNDR at output, interfering signals at front-end input -25dBm, at 5MHz offset and -5MHz offset and modulated as in 3GPP, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, production tested by measurement of SNDR at output on CW input signal at -69dBm, SNDR at MAX-PHY filter output established with FFT		-92		dBm

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band IV and X Downlink WCDMA Rx Mode on RXIN5 (Monitor) (continued)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb4fd-8	Sensitivity with Intermodulation Interference 3GPP TS25.101 Section 7.8.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity, interfering signals at front-end input -46dBm, at 10MHz offset (CW) and 20MHz offset (modulated) as in 3GPP, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, production tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-109		dBm
Wb4fd-10	Spurious Emissions Out-of-Band 3GPP TS25.101 Section 7.9.1	30MHz to 12750MHz in 100kHz bandwidth (Note 3)		-80	-60	dBm
Wb4fd-11	Spurious Emissions in Receive Bands 3GPP TS25.101 section 7.9.2	Front-end assumed response as above, 1710MHz to 1785MHz and 2110MHz to 2170MHz (Note 3)		-93	-80	dBm
Wb4fd-12	Conversion Gain High LNA Gain	LNA gain high, PGA gain register set to 11, tested on CW input signal at -90dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	34	42		dB
Wb4fd-13	Conversion Gain Low LNA Gain	LNA gain low, PGA gain register set to 0, tested on CW input signal at -20dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output		-12	-8	dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Downlink WCDMA RX MODE on RXIN2 (Monitor)

Assumed External Front-End Filtering Characteristics Between Antenna and LNA:

BAND (MHz)	Downlink 1800 to 1880	1 to 1750	1750 to 1770	1770 to 1815	1864 to 1930	1930 to 1950	1950 to 12750
ATTENUATION (dB)	Attenuation	Minimum Attenuation (dB)					
	2	15	10	0	0	10	15

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb9fd-0	Frequency Band		1807.4		1877.4	MHz
Wb9fd-1	Sensitivity 3GPP TS25.101 Section 7.3.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity, using UL reference measurement channel, (12.2kbps) as specified in C.3.1 3GPP, 25.101, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-110	-101	dBm
Wb9fd-4	Sensitivity with Adjacent Channel Interference 3GPP TS25.101 Section 7.5.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity, interfering signals at front-end input -52dBm, at 5MHz offset and -5MHz offset and modulated as in 3GPP, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, production tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-109		dBm
Wb9fd-4a	Sensitivity with Adjacent Channel Interference 3GPP TS25.101 Section 7.5.1 CASE 2	LNA gain medium, PGA gain register set to 6, tested SNDR at output, interfering signals at front-end input -25dBm, at 5MHz offset and -5MHz offset and modulated as in 3GPP, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, production tested by measurement of SNDR at output on CW input signal at -69dBm, SNDR at MAX-PHY filter output established with FFT		-94		dBm

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Downlink WCDMA RX MODE on RXIN2 (Monitor) (continued)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb9fd-8	Sensitivity with Intermodulation Interference 3GPP TS25.101 Section 7.8.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity, interfering signals at front-end input -46dBm, at 10MHz offset (CW) and 20MHz offset (modulated) as in 3GPP, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, production tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-109		dBm
Wb9fd-10	Spurious Emissions Out-of-Band 3GPP TS25.101 Section 7.9.1	30MHz to 12750MHz in 100kHz bandwidth (Note 3)		-60	-55	dBm
Wb9fd-11	Spurious Emissions in Receive Bands 3GPP TS25.101 section 7.9.2	Front-end assumed response as above, 1750MHz to 1785MHz and 1845MHz to 1880MHz (Note 3)		-97	-80	dBm
Wb9fd-12	Conversion Gain High LNA Gain	LNA gain high, PGA gain register set to 11, tested on CW input signal at -90dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	37	45		dB
Wb9fd-13	Conversion Gain Low LNA Gain	LNA gain low, PGA gain register set to 0, tested on CW input signal at -20dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output		-12.5	-8	dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

PCS Band GMSK Rx Mode on RXIN2

Assumed External Front-End Filtering Characteristics Between Antenna and LNA

BAND (MHz)	In-Band 1930 to 1990	(a) 1 to 1910	(b) 2010 to 2050	(c) 2230 to 2255	(d) 2255 to 12750
ATTENUATION (dB)	Attenuation	Minimum Attenuation			
	3.5	15	6	6	15

DCS Band Rx Mode on RXIN2

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
pcs-0	RF Frequency	At pin RXIN2, 200kHz channel raster, lowest to highest channel center frequency	1930.2		1994.8	MHz
pcs-1	Sensitivity 3GPP TS100.910 Section 6.2	LNA gain high, PGA gain register set to 12, assumed SNDR > 7dB at sensitivity, using static E-TCH/F as specified in 3GPP TS 100.910, production tested by measurement of SNDR at output on CW input signal at -102dBm, SNDR at MAX-PHY filter output established with FFT		-109	-101	dBm
pcs-10	Conversion Gain High LNA Gain	LNA gain high, PGA gain register set to 12, production tested on CW input signal at -102dBm, calculated by subtracting the FE input signal in dBm from the output signal in dBFS at digital filter outputs, includes digital gain to the16-bit output	45	50		dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Antenna—Downlink Port (Applies to Downlink WCDMA Rx Mode on RXIN4)

BAND (MHz)	Downlink 869 to 894	1 to 804	914 to 2200	2230 to 2255	2255 to 12750
ATTENUATION (dB)	Attenuation	Minimum Attenuation			
	2.5	32	32	6	15

Band V Downlink WCDMA Rx Mode on RXIN4 (Monitor)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb5fd-0	Frequency Band		867.4		891.6	MHz
Wb5fd-1	Sensitivity 3GPP TS25.101 Section 7.3.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-111.5	-104.7	dBm
Wb5fd-4	Sensitivity with Adjacent Channel Interference 3GPP TS25.101 Section 7.5.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity; interfering signals at front-end input -52dBm, at 5MHz offset and -5MHz offset and modulated as in 3GPP, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-111	-101	dBm
Wb5fd-9	Spurious Emissions Out-of-Band 3GPP TS25.101 Section 7.9.1 (Note 3)	30MHz to 1000MHz, 100kHz bandwidth (Note 3)		-100	-60	dBm
		1000MHz to 12750MHz, 1MHz bandwidth (Note 3)		-90	-50	

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band V Downlink WCDMA Rx Mode on RXIN4 (Monitor) (continued)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb5fd-10	Spurious Emissions in Receive Bands 3GPP TS25.101 Section 7.9.2	Front-end assumed response as above, 824MHz to 849MHz and 869MHz to 894MHz (Note 3)		-100	-80	dBm
Wb5fd-11	Conversion Gain High LNA Gain	LNA gain high, PGA gain register set to 11, tested on CW input signal at -90dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	40	45		dB
Wb5fd-12	Conversion Gain Low LNA Gain	LNA gain low, PGA gain register set to 0, tested on CW input signal at -20dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the16-bit output		-13	-8.5	dB

GSM850 Band RX Mode

The signal shares the same path as WCDMA Band V downlink. Losses applied are:

1) Diplexer: 0.3dB
2) Band V duplexer, antenna to downlink port (same as WCDMA table)
3) SPDT: 0.3dB

GSM850 Band GMSK Monitor on RXIN4

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
G850-0	RF Frequency		865.2		893.8	MHz
G850-1	Sensitivity 3GPP TS100.910 Section 6.2	LNA gain high, PGA gain register set to 12, assumed SNDR > 7dB at sensitivity;,using static E-TCH/F as specified in 3GPP TS 100.910, production tested by measurement of SNDR at output on CW input signal at -102dBm;,SNDR at MAX-PHY filter output established with FFT		-110		dBm

Tx MODE AC ELECTRICAL CHARACTERISTICS

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
W1	RF Frequency Range	Center of the WCDMA signal, Bands IV and X output (TXOUT)	2112.4		2167.6	MHz
		Center of the WCDMA signal, Bands III and IX output (TXOUT)	1807.4		1877.4	
W2	Linear Output Power	TX_GAIN = 1023	0			dBm
W3	Adjacent Channel Power Ratio	Offset frequency = ±5MHz in 3.84MHz BW		-55		dBc
W4	Alternate Channel Power Ratio	Offset frequency = ±10MHz in 3.84MHz BW		-70		dBc
W5	Rx Band Noise Power, $P_{OUT} \leq$ 0dBm (Note 3)	Noise measured at -400MHz offset in 3.84MHz BW, then convert to per Hz, Band IV and X output		-149	-142	dBm/Hz
		Noise measured at -95MHz offset in 3.84MHz BW, then convert to per Hz, Band III and IX output		-145	-139	
W6	EVM	P_{OUT} = 0dBm		3.8		%
W6a	RCDE	TM6, 8 channels at 0dBm		-28		dB
W7	Minimum Output Power	TX_GAIN = 0		-62	-47	dBm
W8	Output Power Deviation from T_A = +25°C to -40°C (Note 3)	TX_GAIN = 1023		0.8	2.9	dB
W9	Output Power Deviation from T_A = +25°C to +85°C (Note 3)	TX_GAIN = 1023	-3	-0.7		dB
W10	Power Control Step Size Accuracy (1dB)	Five calibration points over the power control range to create four linear regions, any linearly interpolated 1dB TX_GAIN step over the specified power range (W2 and W7) produces 1dB output power step within this error range		±0.25		dB
W11	Power Control Step Size Accuracy (10dB)	Five calibration points over the power control range to create four linear regions, any linearly interpolated 10dB TX_GAIN step over the specified power range (W2 and W7) produces 10dB output power step within this error range		±0.75		dB

AC ELECTRICAL CHARACTERISTICS: GENERAL

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE FREQUENCY INPUT						
R1	Input Level	Test condition	125		600	mV_{P-P}
R2	Input Frequency	Reference divider set to divide-by-2 for frequencies higher than 26MHz	13	19.2	40	MHz
REFERENCE FREQUENCY OUTPUT						
RO1a	REFOUT Output Level, AC	500Ω ll 22pF load, REFOUT_LV_CMOS_SEL = 1	110	320	500	mV_{P-P}
RO1b	REFOUT Output Level, DC			0.8		V
RO2	REFOUT Output Amplitude	500Ω ll 22pF load, REFOUT_LV_CMOS_SEL = 0	2.25	2.7		V_{P-P}
RO4	REFOUT Output Frequency	Matches REFIN frequency (FREF)	13	19.2	40	MHz
Rx DIGITAL LOW-VOLTAGE DIFFERENTIAL SIGNALING OUTPUT INTERFACE						
LV0	Output Bit Rate on Each I and Q	Test condition		153.6		Mbps
LV1	Output Common Mode Voltage			1.2		V
LV3	Output Differential Swing on Load (Note 3)	120Ω differential output load (Note 3)	100	140	220	mV_{PEAK}
LV4	Differential Output Resistance			670		Ω
Tx BASEBAND INTERFACE						
Bb1	Input Bit Rate, on Each I and Q	Test condition		153.6		Mbps
Bb8	Common-Mode Input Voltage			1.25		V
Bb9	Differential Input Swing		112	140	500	mV_{P-P}
Bb10	Differential Input Resistance (Note 3)	Bit TXINDACZI = 1	55	100	140	Ω
Bb11		Bit TXINDACZI = 0	140	220	340	
Rx RF PLL						
RS1	Valid RF Main Division Ratio Range		65		169	
RS3	Valid Main Fractional Divider Programming Value	20-bit resolution	00000		FFFFF	hex
RS5	Charge-Pump Current Gain	Using 800µA setting	0.5	0.82	1.0	mA
RS6a	VCO Tuning Gain	RXVCO, high band	38	127	216	MHz/V
RS6b		RXVCO, low band	21	65	111	
RS9	PLL Settling Time	50kHz loop bandwidth		30		µs

AC ELECTRICAL CHARACTERISTICS: GENERAL (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Tx RF PLL						
TS2	Valid RF Main Division Ratio Range		69		167	
TS3	Valid Reference Division Ratios	Division ratios are 1 or 2	1		2	
TS4	Valid Main Fractional Divider Programming Value	20-bit resolution	00000		FFFFF	hex
TS5	Charge-Pump Current CP	800µA	0.5	0.82	1.0	mA
TS9	PLL Settling Time	50kHz loop bandwidth		30		µs
DAC1	Resolution	Monotonicity is production tested		12		Bits
AFC DAC						
DAC3	Output-Voltage High	Load > 200kΩ to GND, AFCDAC = all 1	2.55	2.68		V
DAC4	Output-Voltage Low	Load > 200kΩ to $V_{CC\_}$, AFCDAC = all 0		0.37	0.45	V
DAC6	Settling Time	Step from 0.6V to 2V, settling to ±10mV		1		µs
DIGITAL TEMPERATURE SENSOR						
T1	Output Code vs. Temperature	T_A = -40°C		5		°/code
T2		T_A = +25°C		17		
T3		T_A = +85°C		27		°/code
T5	Code Slope	T_A = -20°C to +70°C		5		
ISOLATION						
M1	RXIN_ Pin-to-Pin Isolation	Between any RXIN_ pins, with one of the two ports disabled		30		dB
M2	TXOUT_ to RXIN_ Isolation	Between any TXOUT and RXIN_, with both ports on		60		dB

Note 2: Production tested at T_A = +25°C. Cold and hot are guaranteed by design and characterization.
Note 3: Guaranteed by design and characterization.

General Comments

MAX-PHY

MAX-PHY is Maxim's solution for the digital interface system between the radio IC and the baseband/DSP. It is a multimode, software-programmable, digital signal post-processing engine that processes the data out of the radio IC and produces the digital filtered outputs for use in the DSP. It enables multimode operation of the radio through software control. Maxim offers an evaluation kit for the MAX2552 along with an FPGA-based MAX-PHY evaluation platform. The FPGA includes the recommended digital channel-selection filters. The Verilog code for these filters is also available for integration into the DSP. Contact Maxim for further information.

Additional Information

The specifications in the following pages calculate sensitivity with a specified front-end loss from a measured signal-to-noise and distortion ratio (SNDR) and an assumed minimum output $SNDR_{SENS}$ needed for demodulation at sensitivity. The sensitivity values can be related to noise figure by the formula:

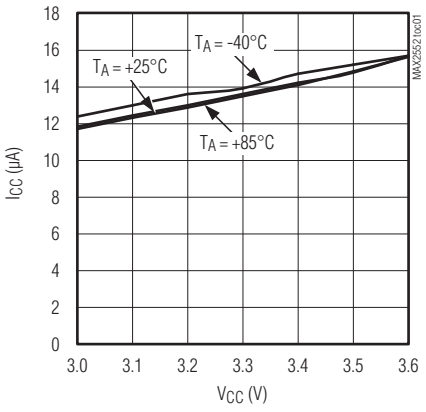
Noise Figure of MAX2552 (dB) = Sensitivity (dBm) - Front-End Loss (dB) - $SNDR_{SENS}$ (dB) + 174dBm/Hz - 10 x LOG(bandwidth in Hz)

Low-noise amplifier (LNA) and programmable-gain amplifier (PGA) gain are set according to the Conditions column in the *Electrical Characteristics* tables. The output SNDR is measured using MAX-PHY and the bandwidth of the measurement is defined by the digital filters in MAX-PHY. DC at the output is excluded from the SNDR measurement. SNDR is calculated using an FFT of the output bytes with a typical FFT length of 2^{14} output samples.

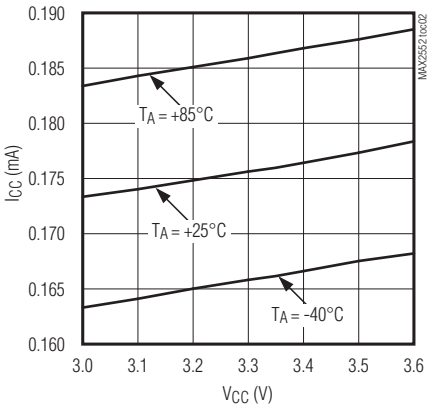
Typical Operating Characteristics

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

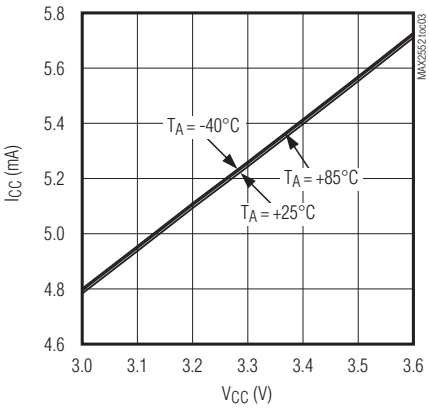
SLEEP MODE I_{CC}



AFC-ONLY MODE I_{CC}



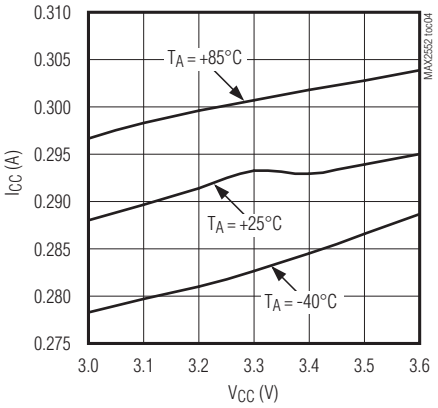
REFERENCE BUFFER MODE I_{CC}



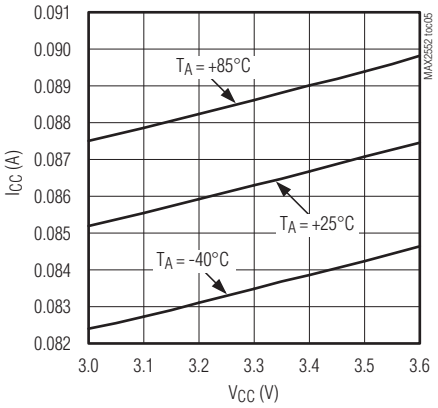
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

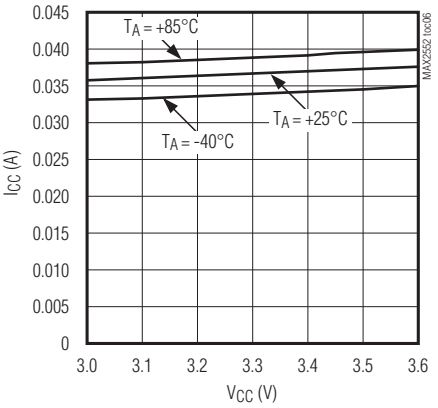
BAND4 FULL DUPLEX MODE I_{CC}



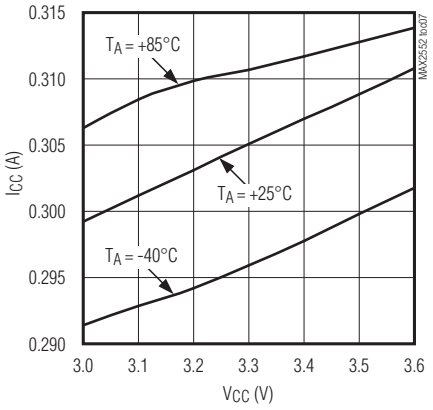
BAND4 RX ONLY MODE I_{CC}



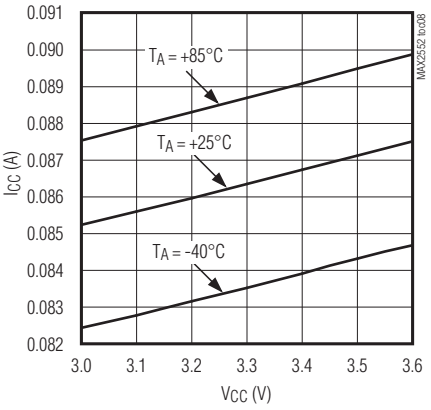
BAND4 RX IDLE MODE I_{CC}



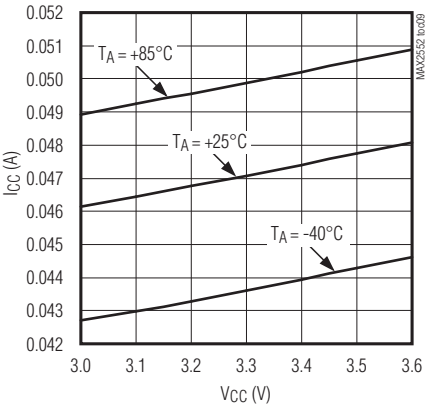
BAND9 FULL DUPLEX MODE I_{CC}



BAND9 RX ONLY MODE I_{CC}



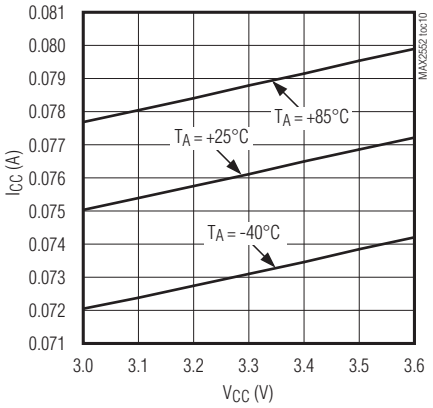
BAND9 RX IDLE MODE I_{CC}



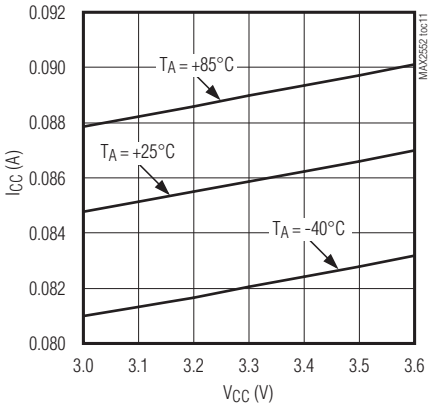
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

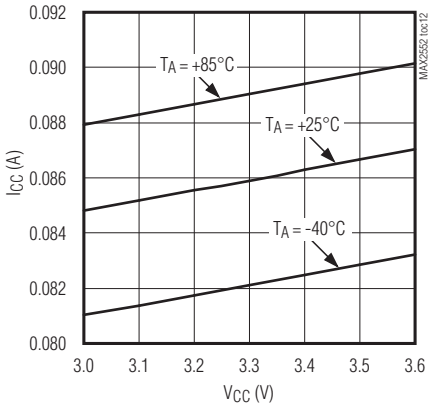
BAND4 RX MONITOR MODE I_{CC}



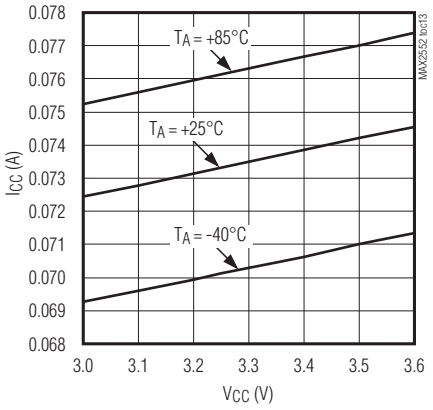
BAND9 RX MONITOR MODE I_{CC}



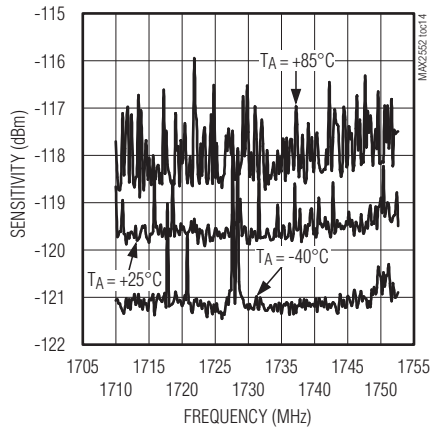
PCS MONITOR MODE I_{CC}



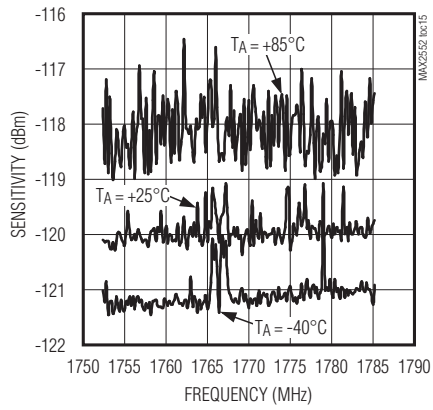
GSM MONITOR MODE I_{CC}



BAND4 UPLINK RX1 SENSITIVITY



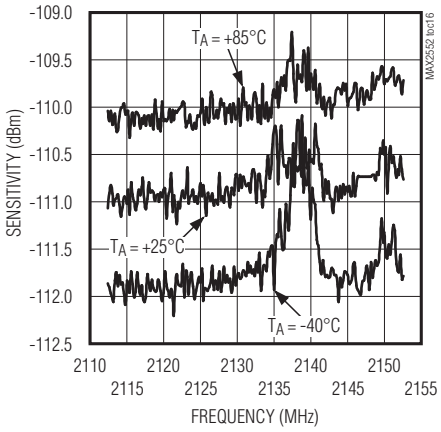
BAND9 UPLINK RX1 SENSITIVITY



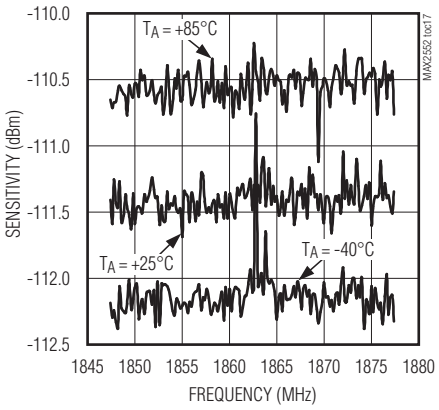
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

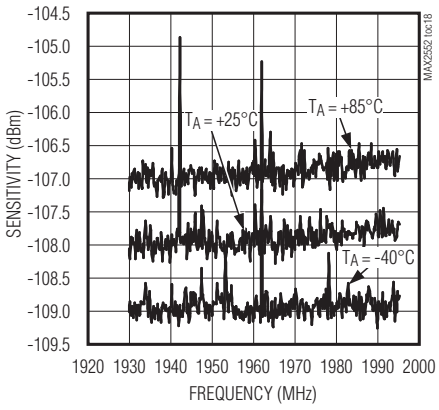
BAND4 DOWNLINK RX5 SENSITIVITY



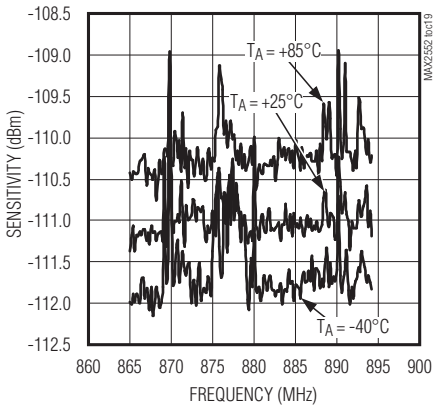
BAND9 DOWNLINK RX2 SENSITIVITY



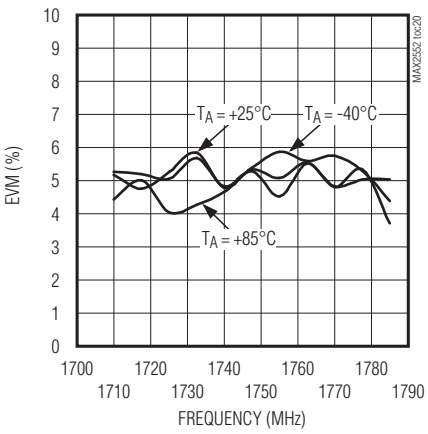
PCS RX2 SENSITIVITY



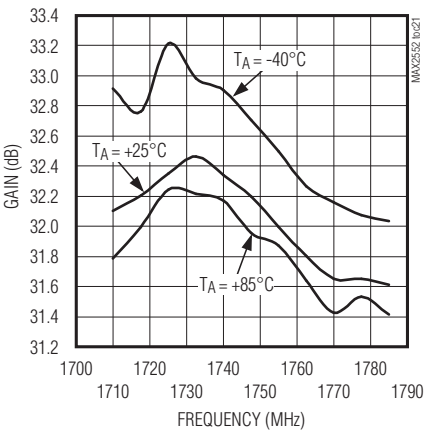
GSM RX4 SENSITIVITY



BAND#4 AND BAND#9 UPLINK RX1 EVM



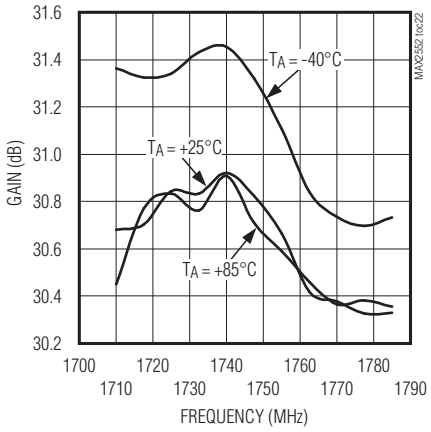
RX1 GAIN, LNA = HIGH, PGA = 6



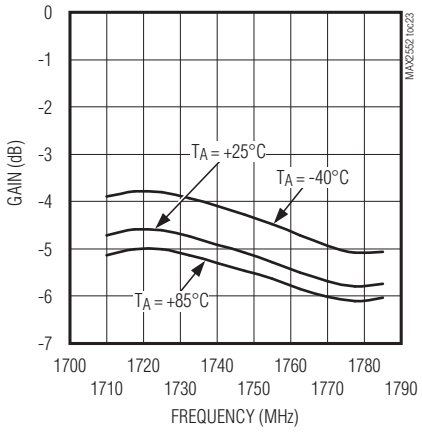
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

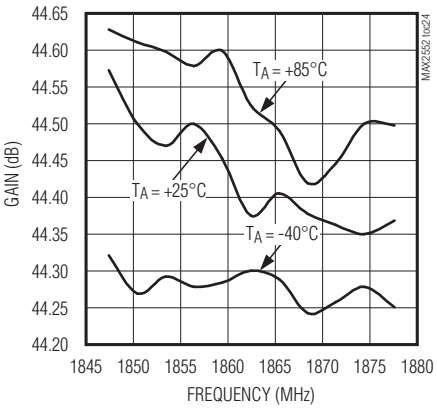
RX1 GAIN, LNA = MID, PGA = 9



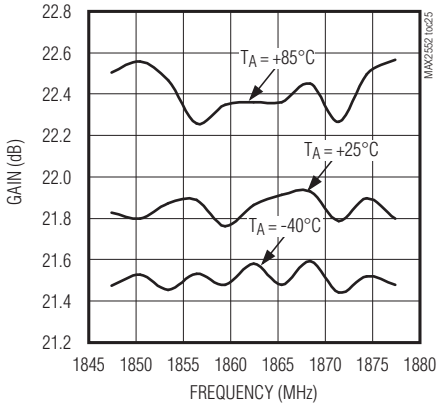
RX1 GAIN, LNA = LOW, PGA = 1



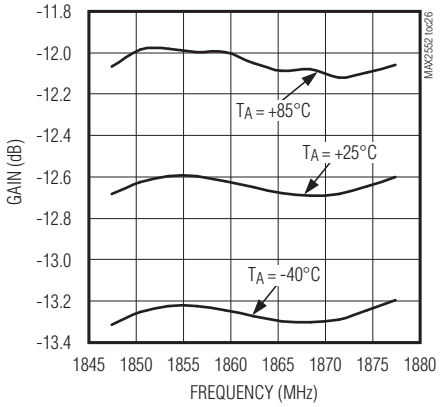
RX2 GAIN, LNA = HIGH, PGA = 11



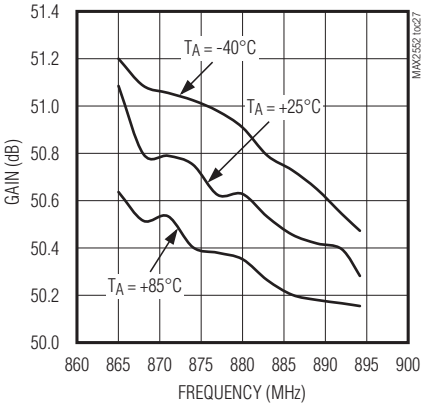
RX2 GAIN, LNA = MID, PGA = 6



RX2 GAIN, LNA = MIN, PGA = 0



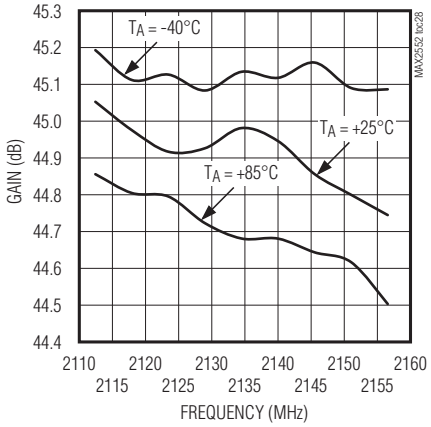
RX4 GAIN, LNA = HIGH, PGA = 12



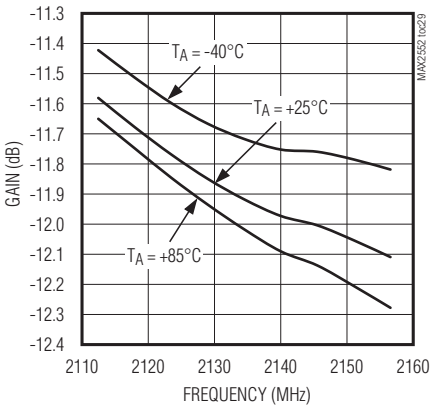
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

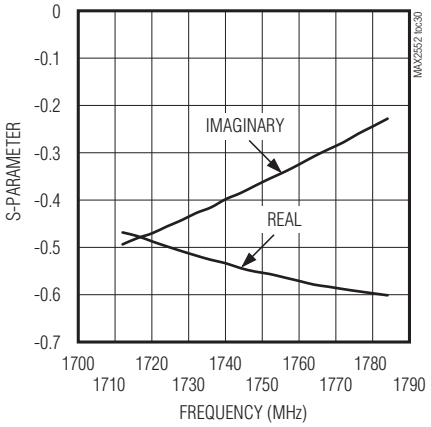
RX5 GAIN, LNA = HIGH, PGA = 11



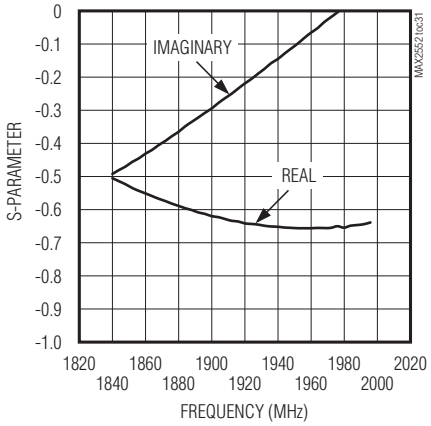
RX5 GAIN, LNA = LOW, PGA = 0



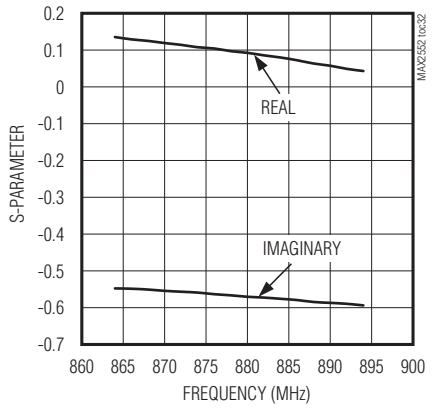
RXIN1 PIN S-PARAMETER



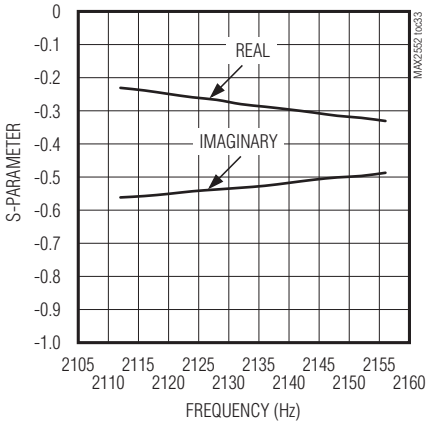
RXIN2 PIN S-PARAMETER



RXIN4 PIN S-PARAMETER



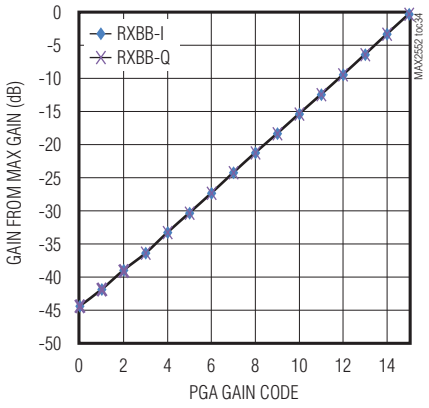
RXIN5 PIN S-PARAMETER



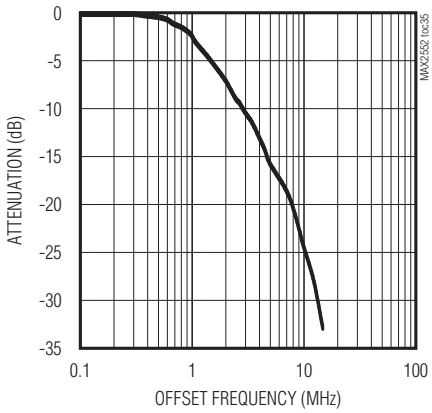
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

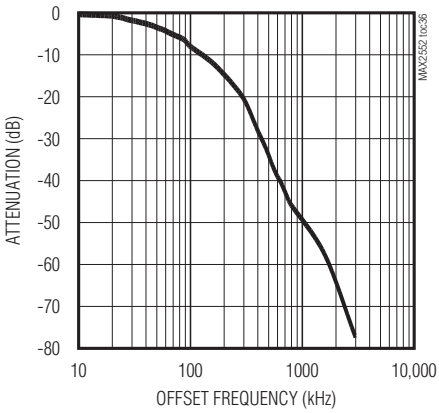
RX GAIN vs. PGA GAIN CODE



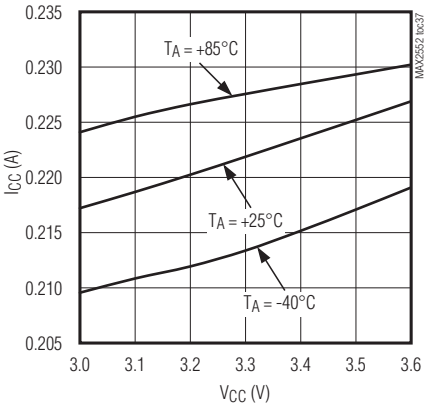
WCDMA FILTER RESPONSE vs. OFFSET FREQUENCY



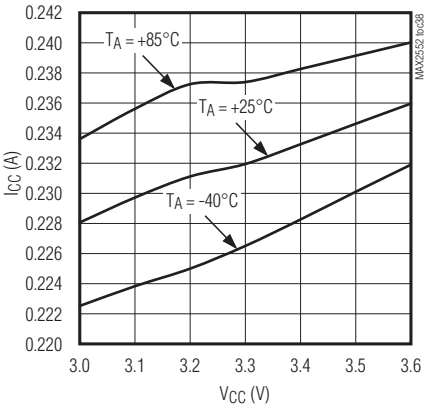
GSM FILTER RESPONSE vs. OFFSET FREQUENCY



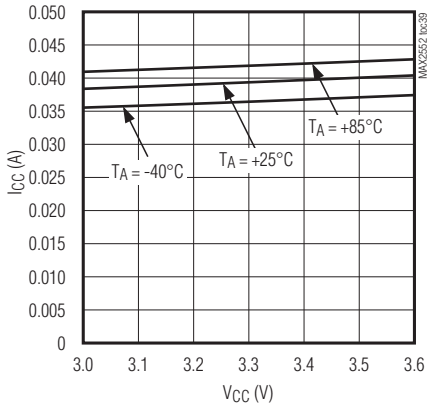
BAND4 TX ONLY MODE I_{CC}



BAND9 TX ONLY MODE I_{CC}



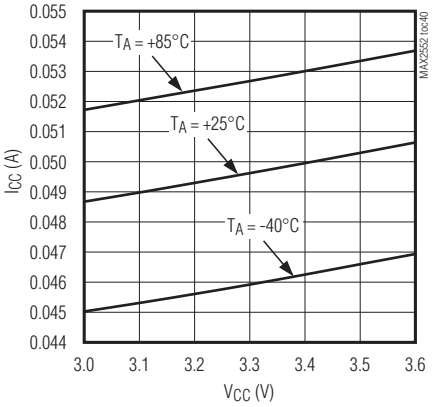
BAND4 TX IDLE MODE I_{CC}



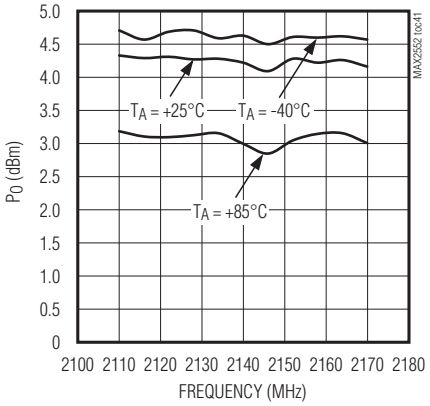
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

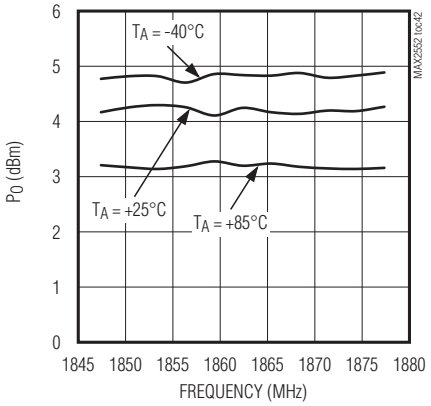
BAND9 TX IDLE MODE I_{CC}



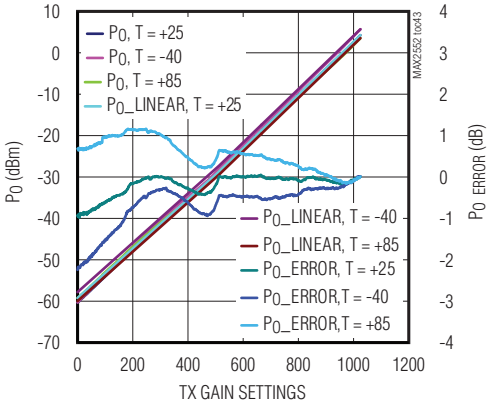
TX MAXIMUM OUTPUT POWER, BAND4



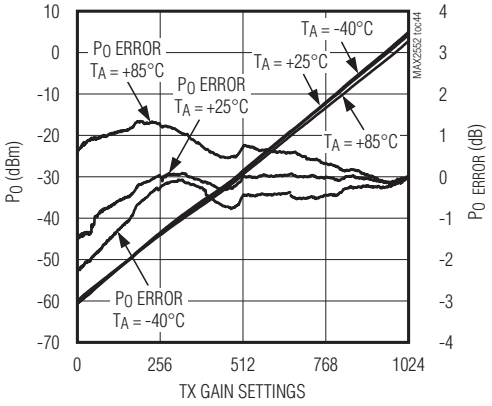
TX MAXIMUM OUTPUT POWER, BAND9



TX OUTPUT POWER vs. GAIN SETTING, BAND4



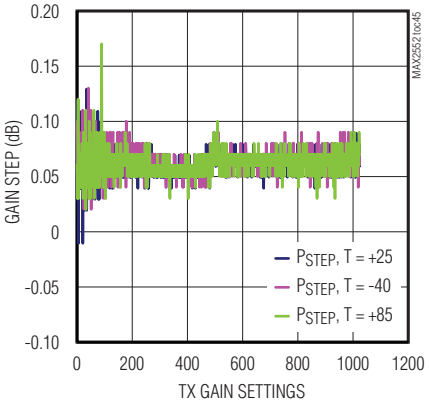
TX OUTPUT POWER vs. GAIN SETTINGS, BAND9



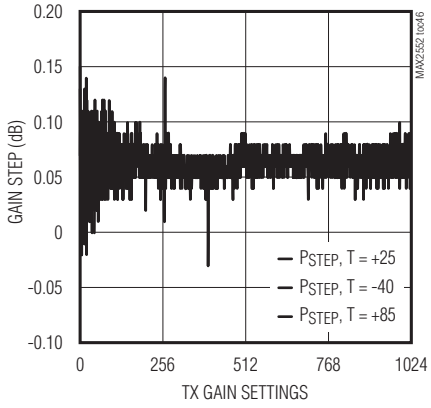
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

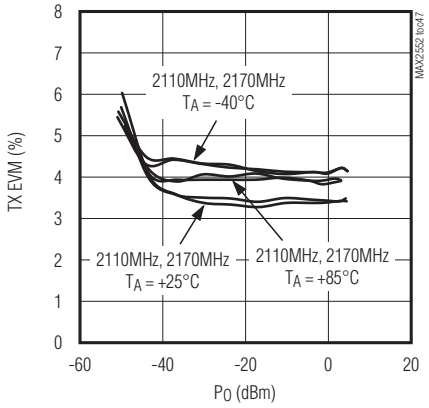
TX GAIN STEP vs. GAIN SETTINGS, BAND4



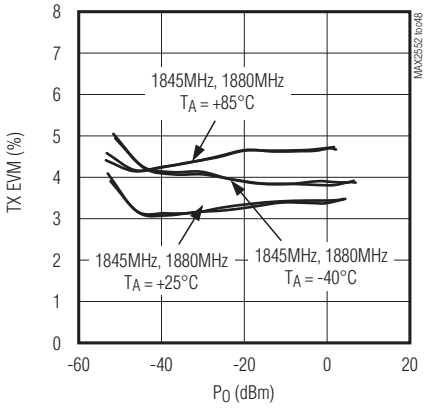
TX GAIN STEP vs. GAIN SETTINGS, BAND9



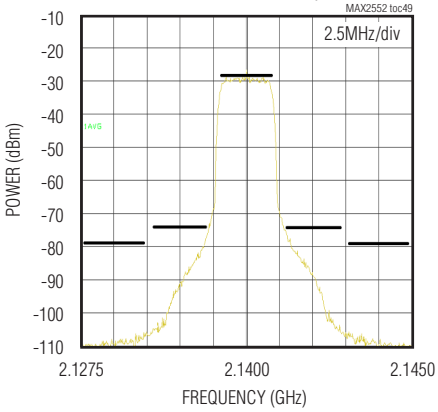
TX EVM, BAND4



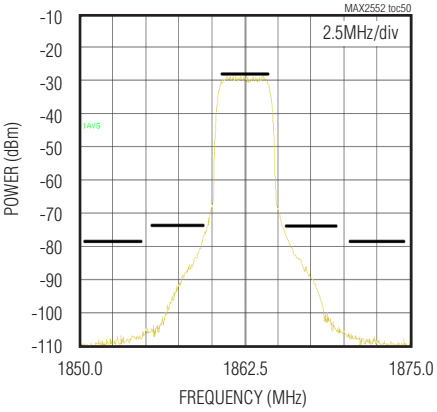
TX EVM, BAND9



TX OUTPUT SPECTRUM , BAND4



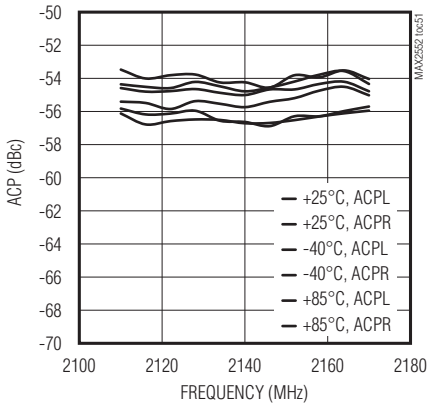
TX OUTPUT SPECTRUM , BAND9



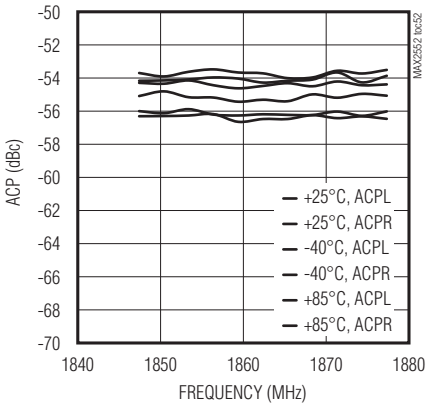
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

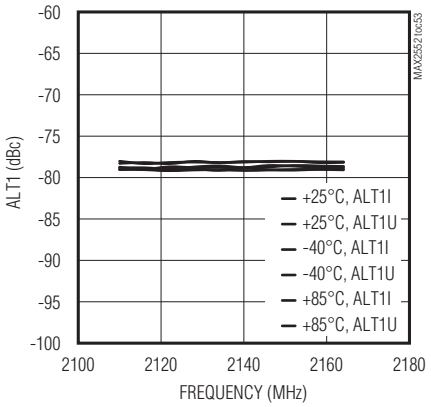
ADJACENT CHANNEL POWER RATIO AT 0dBm, BAND4



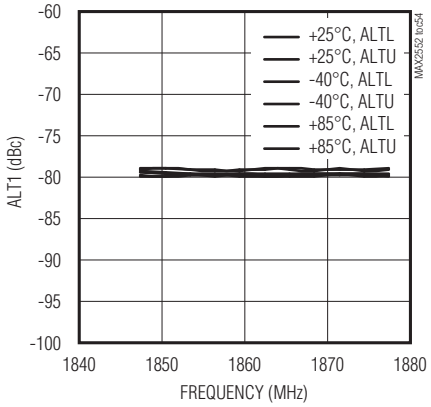
ADJACENT CHANNEL POWER RATIO AT 0dBm, BAND9



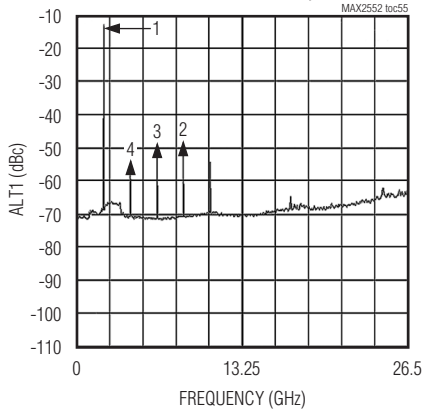
ALTERNATE CHANNEL POWER RATIO AT 0dBm, BAND4



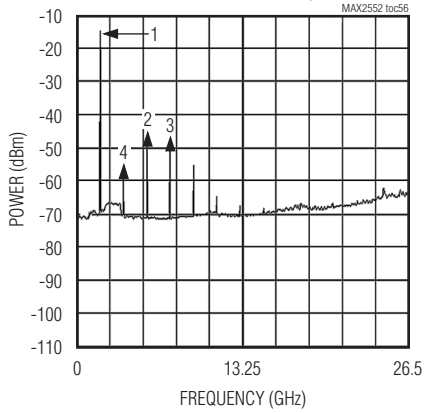
ALTERNATE CHANNEL POWER RATIO AT 0dBm, BAND9



TX OUTPUT SPECTRUM, BAND4



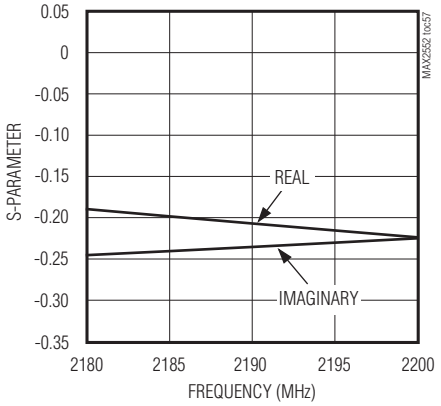
TX OUTPUT SPECTRUM, BAND9



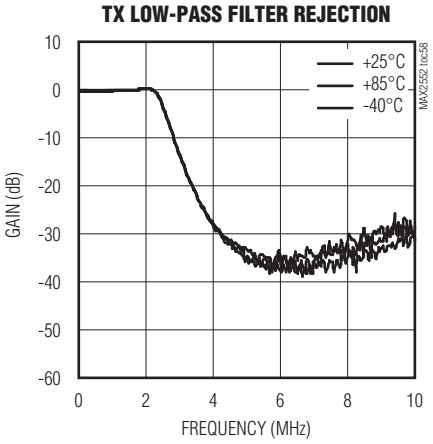
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

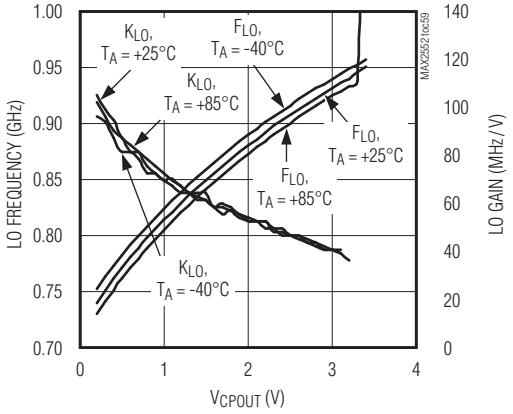
TXOUTH PIN S-PARAMETER, HIGH BAND



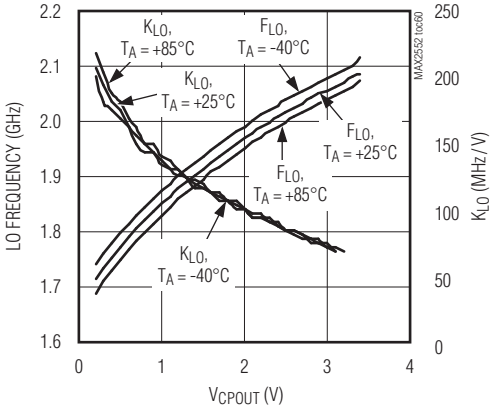
TX LOW-PASS FILTER REJECTION



LO FREQUENCY AND GAIN WITH REG3<20:19> OR REG28<15:14> = 01



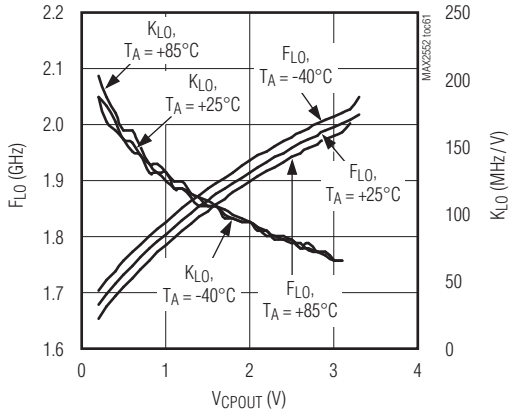
LO FREQUENCY AND GAIN WITH REG3<20:19> OR REG28<15:14> = 10, AND REG3<22:21> OR REG28<17:16> = 00



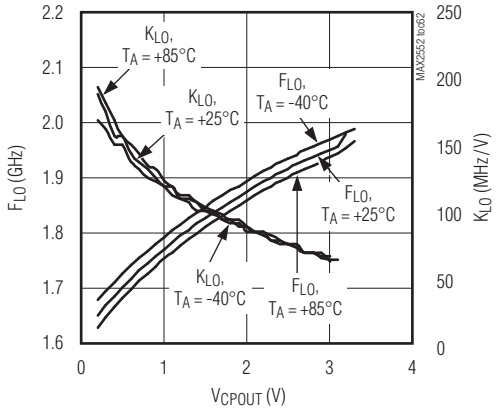
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

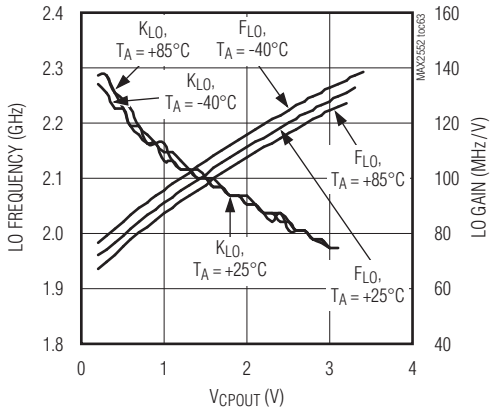
LO FREQUENCY AND GAIN WITH REG3<20:19> OR REG28<15:14> = 10, AND REG3<22:21> OR REG28<15:14> = 01



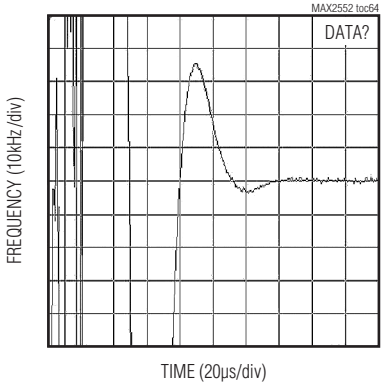
LO FREQUENCY AND GAIN WITH REG3<20:19> OR REG28<15:14> = 10, AND REG3<22:21> OR REG28<15:14> = 11



LO FREQUENCY AND GAIN WITH REG3<20:19> OR REG28<15:14> = 11



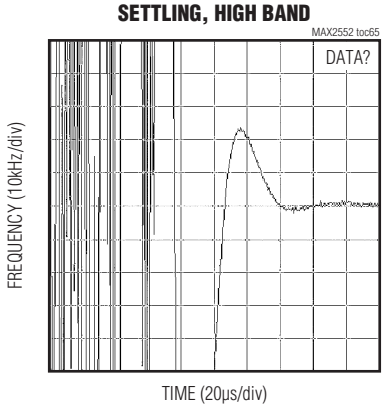
TURN-ON FREQUENCY SETTLING, HIGH BAND



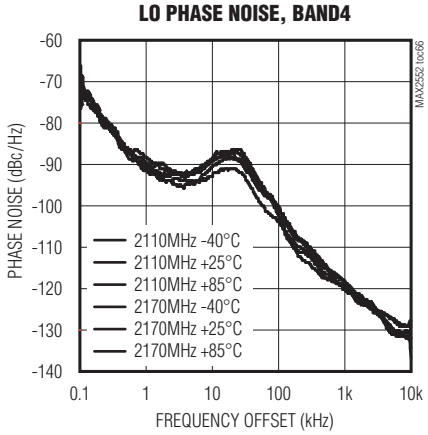
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

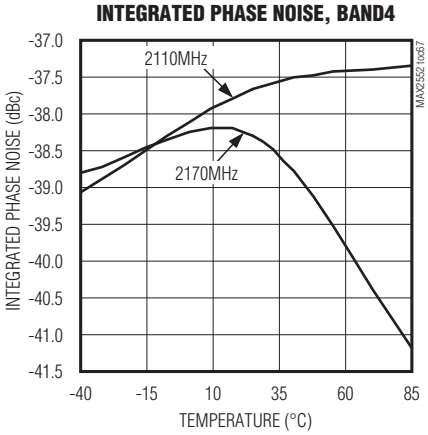
CHANNEL-SWITCH FREQUENCY SETTLING, HIGH BAND



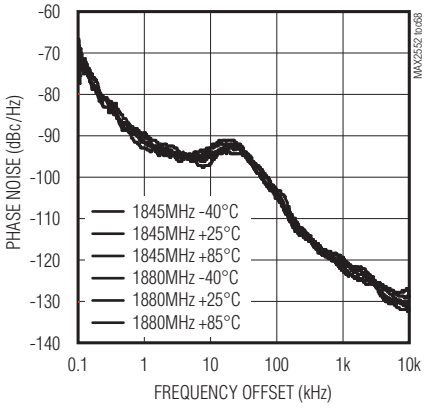
LO PHASE NOISE, BAND4



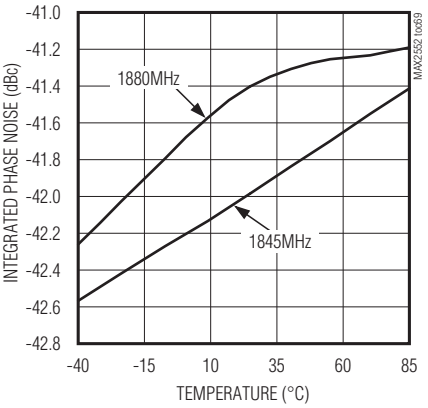
INTEGRATED PHASE NOISE, BAND4



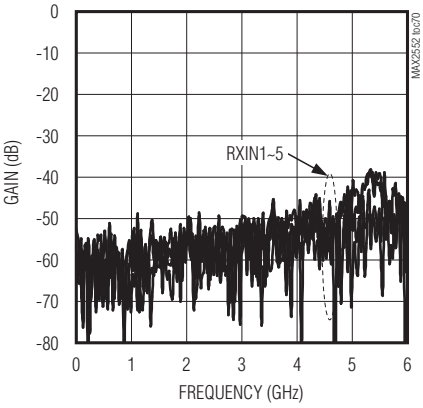
LO PHASE NOISE, BAND9



INTEGRATED PHASE NOISE, BAND9



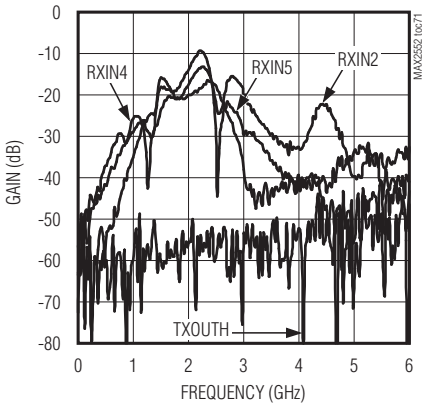
GAIN FROM TXOUTH TO OTHER RF PORTS



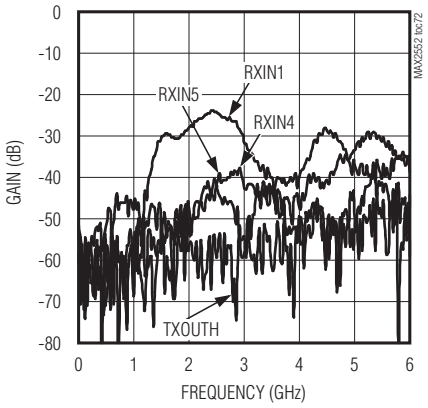
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

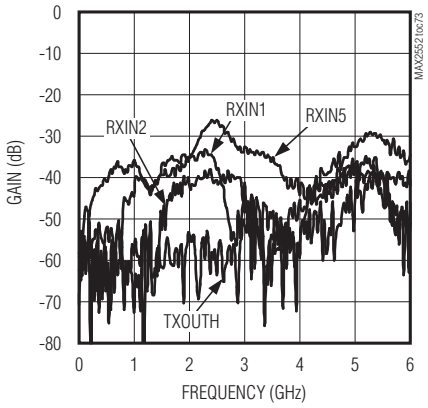
GAIN FROM OTHER RF PORTS TO RXIN1



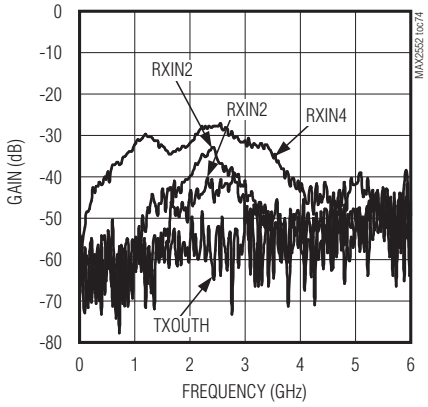
GAIN FROM OTHER RF PORTS TO RXIN2



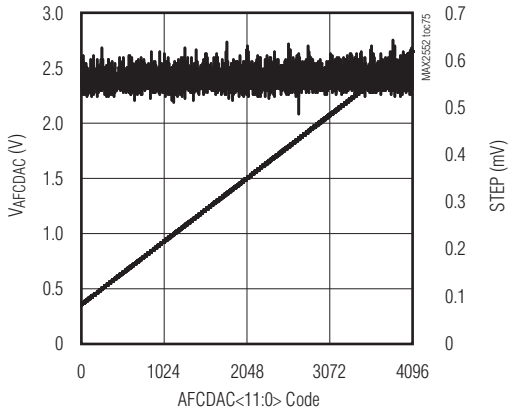
GAIN FROM OTHER RF PORTS TO RXIN4



GAIN FROM OTHER RF PORTS TO RXIN5



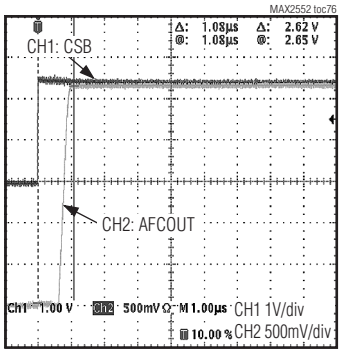
AFCDAC OUTPUT VOLTAGE & STEP



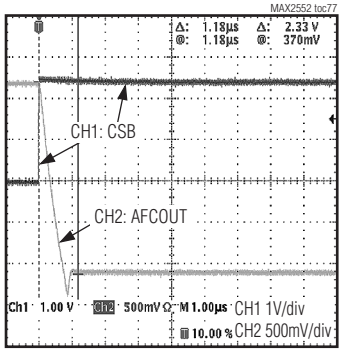
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

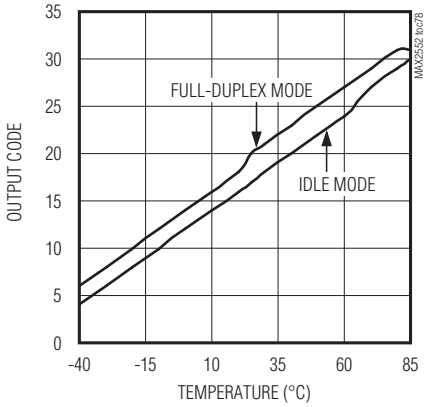
TEMPERATURE SENSOR TURN-ON TRANSIENT



TEMPERATURE SENSOR SWITCHING TRANSIENT FROM CODE 4095 TO 0.

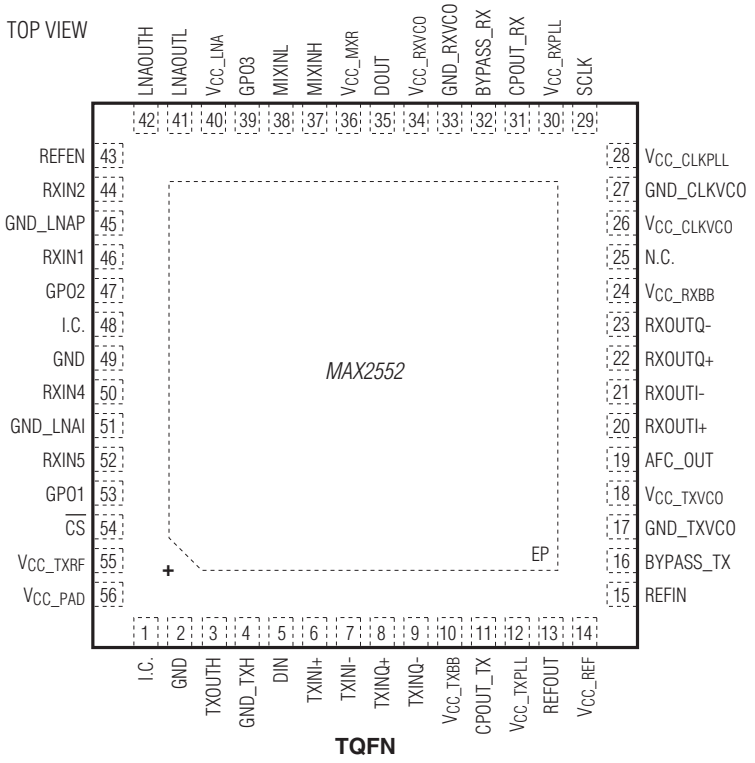


TEMPERATURE SENSOR RESPONSE



Band III, IV, IX, and X WCDMA Femtocell Transceiver with GSM Monitoring

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	I.C.	Internally Connected. Not used.
2	GND	Connect Directly to Ground Plane. Not used.
3	TXOUTH	High-Band TXRF Output. Internally matched to 50Ω over the band of operation.
4	GND_TXH	High-Band Tx Output Ground. Connect directly to ground plane.
5	DIN	Data Input of the 4-Wire Serial Interface
6	TXINI+	Transmitter Noninverting In-Phase Input. Accepts baseband sigma-delta modulated digital bit streams. Connect directly to the baseband processor.
7	TXINI-	Transmitter Inverting In-Phase Input. Accepts baseband sigma-delta modulated digital bit streams. Connect directly to the baseband processor.

Pin Description (continued)

PIN	NAME	FUNCTION
8	TXINQ+	Transmitter Noninverting Quadrature Input. Accepts baseband sigma-delta modulated digital bit streams. Connect directly to the baseband processor.
9	TXINQ-	Transmitter Inverting Quadrature Input. Accepts baseband sigma-delta modulated digital bit streams. Connect directly to the baseband processor.
10	V_{CC_TXBB}	Baseband Tx Path Supply. Connect to a regulated supply voltage. Bypass each supply to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
11	CPOUT_TX	Charge-Pump Output for Tx Synthesizer. Also used as the tuning voltage for Tx VCO. Connect to an external loop filter.
12	V_{CC_TXPLL}	Tx Synthesizer Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
13	REFOUT	Reference Clock Buffer Output. Configurable by the REFEN pin and SPI. See the *REFOUT Functionality* section for details.
14	V_{CC_REF}	Reference Buffer Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
15	REFIN	Reference Input Pin. Connected to TCXO. Requires a DC-blocking capacitor (1nF).
16	BYPASS_TX	Tx VCO Bias Bypass. Bypass to ground with a 470nF capacitor as close as possible.to the pin.
17	GND_TXVCO	Tx VCO Ground. Connect to the PCB ground plane with a separate via.
18	V_{CC_TXVCO}	Tx VCO Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
19	AFC_OUT	AFC DAC Output. The DAC is controlled by the register TXLO_AFCDAC (Table 42).
20	RXOUTI+	Receiver Noninverting In-Phase Output. Digital sigma-delta modulated LVDS output. Connect directly to the baseband processor.
21	RXOUTI-	Receiver Inverting In-Phase Output. Digital sigma-delta modulated LVDS output. Connect directly to the baseband processor.
22	RXOUTQ+	Receiver Noninverting Quadrature Output. Digital sigma-delta modulated LVDS output. Connect directly to the baseband processor.
23	RXOUTQ-	Receiver Inverting Quadrature Output. Digital sigma-delta modulated LVDS output. Connect directly to the baseband processor.
24	V_{CC_RXBB}	Baseband Rx Path Supply. Regulated Power-Supply Input. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
25	N.C.	No Connection. Leave unconnected.
26	V_{CC_CLKVCO}	Clock Generation VCO Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.

Pin Description (continued)

PIN	NAME	FUNCTION
27	GND_CLKVCO	Clock Generation Synthesizer Ground. Connect clock generation synthesizer ground to the PCB ground plane with a separate via.
28	V_{CC_CLKPLL}	Clock Generation Synthesizer Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
29	SCLK	SPI Interface Clock Input. Data is clocked in to the serial-data input on the rising edge of SCLK. See Figure 4 for details.
30	V_{CC_RXPLL}	Rx Synthesizer Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
31	CPOUT_RX	Rx Synthesizer Charge-Pump Output. Also used as the tuning voltage for Rx VCO. Connect to an external loop filter.
32	BYPASS_RX	Rx VCO Bias Bypass. Bypass to ground with a 470nF capacitor as close as possible to the pin.
33	GND_RXVCO	Rx VCO Ground. Connect ground to the PCB ground plane with a separate via.
34	V_{CC_RXVCO}	Rx VCO Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
35	DOUT	SPI Data Output
36	V_{CC_MXR}	Rx Mixer Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
37	MIXINH	High-Band Rx Mixer Input. RF input to mixer from an external filter (optional). Internally DC-blocked and matched to 50Ω.
38	MININL	Low-Band Rx Mixer Input. RF input to mixer from an external filter (optional). Internally DC-blocked and matched to 50Ω.
39	GPO3	General-Purpose Output. Controlled by register 7 (Table 19). GPO3 can also be configured as a PLL lock-detect output.
40	V_{CC_LNA}	LNA Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
41	LNAOUTL	Low-Band LNA Output. RF output from LNA 3 to external SAW filter. Internally DC-blocked and matched to 50Ω.
42	LNAOUTH	High-Band LNA Output. RF Output from LNA 1 to an external SAW filter. Internally DC-blocked and matched to 50Ω.
43	REFEN	Configuration for REFOUT. When REFEN = 0, REFOUT can be configured for CMOS or low-voltage output by the SPI interface. See the *REFOUT Functionality* section. When REFEN = 1, REFOUT is configured as REFIN buffer with CMOS output.
44	RXIN2	Low-Noise Amplifier Input 2. Requires AC-coupling and external matching.
45	GND_LNAP	PCS LNA Ground. Connect directly to ground plane.
46	RXIN1	Low-Noise Amplifier Input 1. Requires AC-coupling and external matching.
47	GPO2	General-Purpose Output. Controlled by register 7<3:2>.

Pin Description (continued)

PIN	NAME	FUNCTION
48	I.C.	Internally Connected. Not used.
49	GND	Connect Directly to Ground Plane. Not used.
50	RXIN4	Low-Noise Amplifier Input 4. Requires AC-coupling and external matching.
51	GND_LNAI	IMT LNA Ground. Connect directly to the ground plane.
52	RXIN5	Low-Noise Amplifier Input 5. Requires AC-coupling and external matching.
53	GPO1	General-Purpose Output. Controlled by register 23[25:24].
54	$\overline{CS}$	Serial-Interface Chip Select. See Figure 4.
55	V_{CC_TXRF}	Tx Upconverter Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
56	V_{CC_PAD}	PA Driver Supply. Connect to a regulated supply voltage. Bypass each supply pin to the PCB ground plane with a capacitor placed as close as possible to the pin. Do not share ground vias among multiple bypass capacitors.
—	EP	Exposed Pad. Connect to a large ground plane to maximize thermal performance.

Detailed Description

Quad RF Inputs

The MAX2552 features four independent RF inputs. RXIN1 is for receiving WCDMA Bands III, IV, IX, and X. Bands II, III, IV, V, IX, and X WCDMA or GSM downlink can be monitored (network listen) by programming the part to receive through the RXIN2, RXIN4, or RXIN5 inputs. This allows the base station to monitor surrounding cells to select the best operating conditions (transmit power, codes, frequency, capacity, etc.)

REFOUT Functionality

The MAX2552 features a reference oscillator buffered output that is configurable by the REFEN input and Register 29. REFOUT can be configured as CMOS or as a low-voltage output. Table 2 lists all REFOUT configurations.

Receiver System Gain Control

The device features programmable-gain LNAs and programmable variable-gain baseband amplifiers, allowing the system gain to be entirely controlled by the serial interface. RX1, RX2, and RX5 have three possible gain states: high gain, medium gain, and low gain. RX4 has high and low gain modes. The gain state of the LNA in operation is programmed by the LNAGAIN bits in the RX_GAIN[15:14] register. Each LNA requires an external matching network to optimize system sensitivity. Table 3, Table 4 and Table 5 provide S11 for each LNA input over the specified band of operation. Table 6 provides S22 of the LNA ouput. The receiver also features a separate dedicated receive path for the 1930MHz to 1995MHz band that enables monitoring.

The baseband amplifiers have 16 possible gain states with each LSB providing a gain step of 3dB. The gain state of the baseband amplifiers is programmed by the PGAGAIN bits in the RX_GAIN[11:8] register. The dynamic range of the data converters when using the recommended sampling rates is sufficient to allow for minimal switching of system gain over varying input signal power.

Table 1. RF Input/Output Frequency Range

PIN	FUNCTION	FREQUENCY RANGE (MHz)
RXIN1	Band III, IV, IX, X WCDMA uplink Rx	1710 to 1785
RXIN2	Band II, III, IX WCDMA monitor	1805 to 1880
RXIN4	Band V downlink WCDMA/GSM monitor	865 to 894
RXIN5	Band IV and X WCDMA monitor	2110 to 2170
TXOUTH	Band IV and X WCDMA downlink Tx	2110 to 2170
TXOUTH	Band III and IX WCDMA downlink Tx	1805 to 1880

Table 2. REFOUT Output Configurations

INPUT			OUTPUT
REFEN INPUT	REFIN_ENOUT3 (TXLO_REF<14>)	REFOUT_LV_CMOS_SEL (TXLO_REF<23>)	OUTPUT TYPE
0	0	X	Off
	1	0	CMOS
		1	Low voltage
1	X	X	CMOS

Table 3. Typical RXIN1 (High Gain) S11 Parameters ($V_{CC\_}$ = +3.3V, T_A = +25°C)

FREQUENCY (MHz)	S11 REAL	S11 IMAGINARY
1710	34.3	-40.1
1715	34.4	-40.0
1720	34.6	-40.0
1725	34.7	-40.0
1730	34.8	-39.9
1735	34.9	-39.9
1740	35.0	-39.9
1745	35.1	-39.8
1750	35.3	-39.8
1755	35.4	-39.8
1760	35.5	-39.8
1765	35.6	-39.8
1770	35.7	-39.8
1775	35.8	-39.8
1780	35.9	-39.8
1785	36.0	-39.8

Table 4. Typical RXIN4 (High Gain) S11 Parameters ($V_{CC\_}$ = +3.3V, T_A = +25°C)

FREQUENCY (MHz)	S11 REAL	S11 IMAGINARY
840	22.0	-53.8
845	22.5	-53.6
850	22.9	-53.4
855	23.3	-53.3
860	23.7	-53.2
865	24.1	-53.1
870	24.3	-53.0
875	24.6	-53.0
880	24.8	-52.9
885	24.9	-52.9
890	25.0	-52.8
895	25.1	-52.8
900	25.1	-52.7
905	25.3	-52.3
910	25.6	-52.2
915	25.9	-52.1
920	26.2	-52.0
925	26.4	-52.0
930	26.5	-51.9
935	26.6	-51.9
940	26.7	-51.8
945	26.8	-51.8
950	26.8	-51.7
955	26.8	-51.6
960	26.8	-51.5
965	26.7	-51.4
970	26.6	-51.2
975	26.5	-51.1
980	26.4	-50.9

Table 5. Typical RXIN5 (High Gain) S11 Parameters ($V_{CC\_}$ = +3.3V, T_A = +25°C)

FREQUENCY (MHz)	S11 REAL	S11 IMAGINARY
2070	16.9	-33.3
2075	16.9	-33.1
2080	17.0	-32.9
2085	17.0	-32.7
2090	17.0	-32.5
2095	17.1	-32.3
2100	17.1	-32.2
2105	17.1	-32.0
2110	17.2	-31.8
2115	17.2	-31.6
2120	17.3	-31.4
2125	17.3	-31.2
2130	17.3	-31.0
2135	17.4	-30.8
2140	17.4	-30.6
2145	17.5	-30.4
2150	17.6	-30.2
2155	17.6	-30.0
2160	17.7	-29.8
2165	17.7	-29.6
2170	17.8	-29.5
2175	17.9	-29.3
2180	17.9	-29.1
2185	18.0	-28.9
2190	18.1	-28.7
2195	18.1	-28.5
2200	18.2	-28.3
2205	18.3	-28.2
2210	18.4	-28.0
2070	16.9	-33.3
2075	16.9	-33.1

Table 6. Typical LNAOUTH (High Gain) S22 Parameters ($V_{CC\_}$ = +3.3V, T_A = +25°C)

FREQUENCY (MHz)	S11 REAL	S11 IMAGINARY
1710	28.2	-5.7
1715	28.5	-5.2
1720	28.8	-4.7
1725	29.1	-4.3
1730	29.4	-3.8
1735	29.7	-3.3
1740	30.0	-2.8
1745	30.3	-2.4
1750	30.6	-1.9
1755	31.0	-1.4
1760	31.3	-0.9
1765	31.6	-0.4
1770	31.9	0.0
1775	32.3	0.5
1780	32.6	1.0
1785	33.0	1.5

Table 7. Typical MIXINH S11 Parameters ($V_{CC\_}$ = +3.3V, T_A = +25°C)

FREQUENCY (MHz)	S11 REAL	S11 IMAGINARY
1710	28.55	-31.48
1715	28.77	-31.50
1720	28.98	-31.53
1725	29.19	-31.56
1730	29.39	-31.60
1735	29.59	-31.64
1740	29.79	-31.69
1745	29.98	-31.75
1750	30.16	-31.81
1755	30.34	-31.87
1760	30.52	-31.94
1765	30.69	-32.01
1770	30.85	-32.09
1775	31.01	-32.17
1780	31.16	-32.26
1785	31.31	-32.35

Digital I/Q Receive Interface

The baseband output of the device is in the form of a digital I/Q interface. The received signals are sampled by a 1-bit sigma-delta modulator clocked at 153.6MHz for WCDMA and 26MHz for GSMK. The digital bitstream out of the converter is transported from the device to the baseband processor by a low-voltage differential signaling (LVDS) interface. The output data is single-bit nonreturn-to-zero (NRZ). The device does not perform any encoding of the data and no clock is exchanged between the device and the baseband processor.

The device performs limited analog filtering only to minimize aliasing; all channel filtering is realized entirely in the digital domain. The digital filtering removes undesired signals as well as the inherent quantization noise of the sigma-delta modulator. In addition, the device's analog filters include a pole at approximately half the channel bandwdith that must be equalized by the digital filters.

The differential outputs require a termination resistor at the digital baseband IC inputs. The output current of the LVDS drivers are programmable by the LVDSI_2X bit in the BB_CLKOUT register to accommodate different termination resistors. Set LVDSI_2X = 1 to set the drive current to nominal for operation with 120Ω differential loads.

Digital I/Q Transmit Interface

The Tx baseband input of the device is in the form of a sigma-delta modulated digital I/Q interface. The digital bitstream of the baseband processor is transported to the device by a low-voltage differential signaling (LVDS) or DDR3 interface. The LVDS signal has a typical common-mode voltage of 1.2V and a differential swing of $140mV_{P-P}$, while DDR3 has a common-mode voltage of 0.75V and differential of $600mV_{P-P}$. For LVDS, the input data should be in single-bit NRZ format; no clock is exchanged between the baseband processor and the device. The device recovers the I/Q bitstreams with an on-chip data recovery circuit. The bitstream is converted to an analog signal and filtered prior to upconversion to an RF signal.

Baseband Input Level

The baseband input is in digital 1-bit sigma-delta converted format. There are internal 1-bit I/Q DACs that restore the level of the incoming digital signals to a repeatable analog level in the device. At a given TX_GAIN value, the RMS output power level depends on the density of the bit stream, not the voltage level of the LVDS digital signal. The density of the bit stream, in turn, depends on the input level of the sigma-delta converter, which resides in the baseband chip. The condition for the AC performance in the EC table calls for -4dBFs peak, which means -4dB relative to the full scale of the input of the sigma-delta converter. The sigma-delta converter, coded in Verilog, and implemented on FPGA has 10 bits (9 bits + sign) at the input. In this case, the full scale is ±511, and -4dBFs peak means ±322 peak excursion. The RMS level is lower than this number, depending on the peak-average ratio of the signal. For TM1, the peak-average is 10.6dB at 0.01%, so the RMS level of the baseband signal is -14.6dBFs, or ±95.

DC Offset

While the inherent DC offset at the I/Q outputs is very low, it is expected that the baseband processor digitally removes any DC offset.

Digital Filters/Sigma-Delta Modulator

Verilog code is available for implementation of the sigma-delta modulator and digital filters in the baseband processor. Contact the factory for more information.

Fractional-N Synthesizers

The device includes three fractional-N frequency synthesizers. One synthesizer is used to generate the receive RF local oscillator (LO), the second is used to generate the transmit RF local oscillator, while the third is used to generate the ADC sampling clock. The loop filter for the ADC sampling clock synthesizer is integrated on-chip. RF synthesizers require an external loop filter. All synthesizers have 20 bits of fractional resolution.

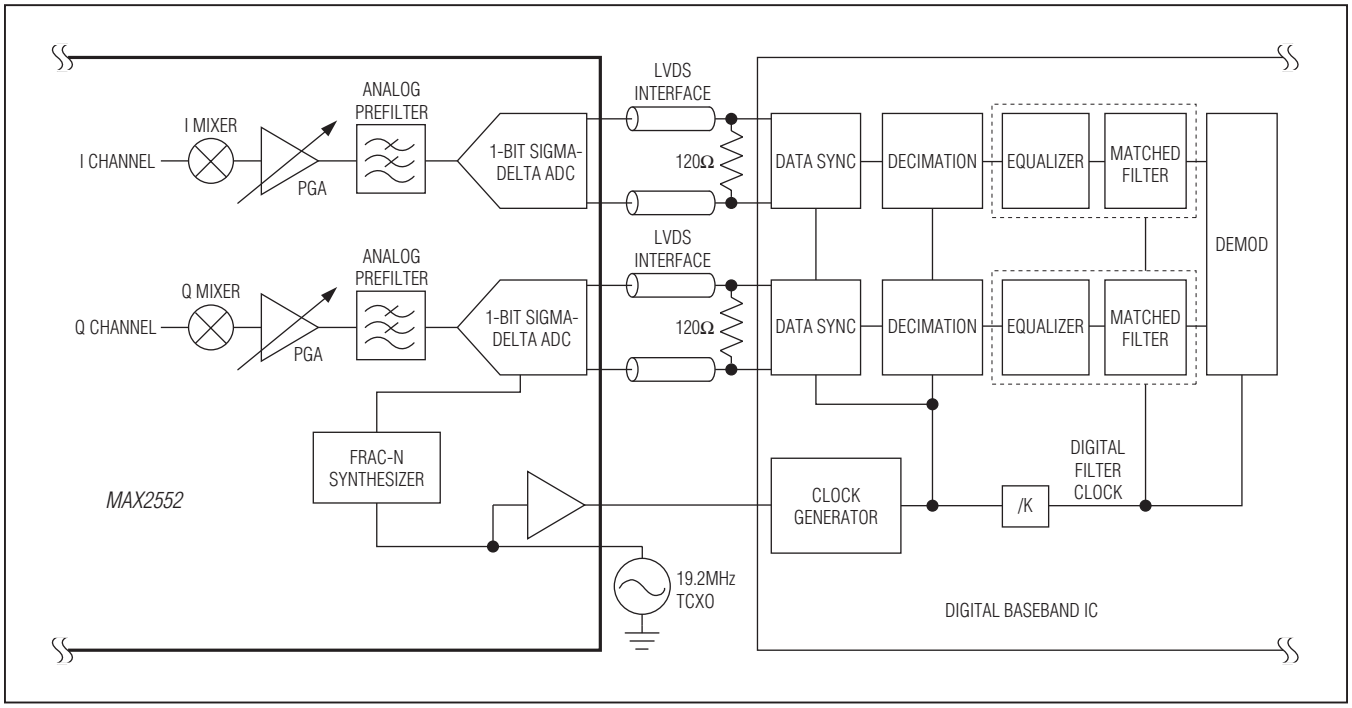


Figure 1. Digital Baseband Receiver Interface

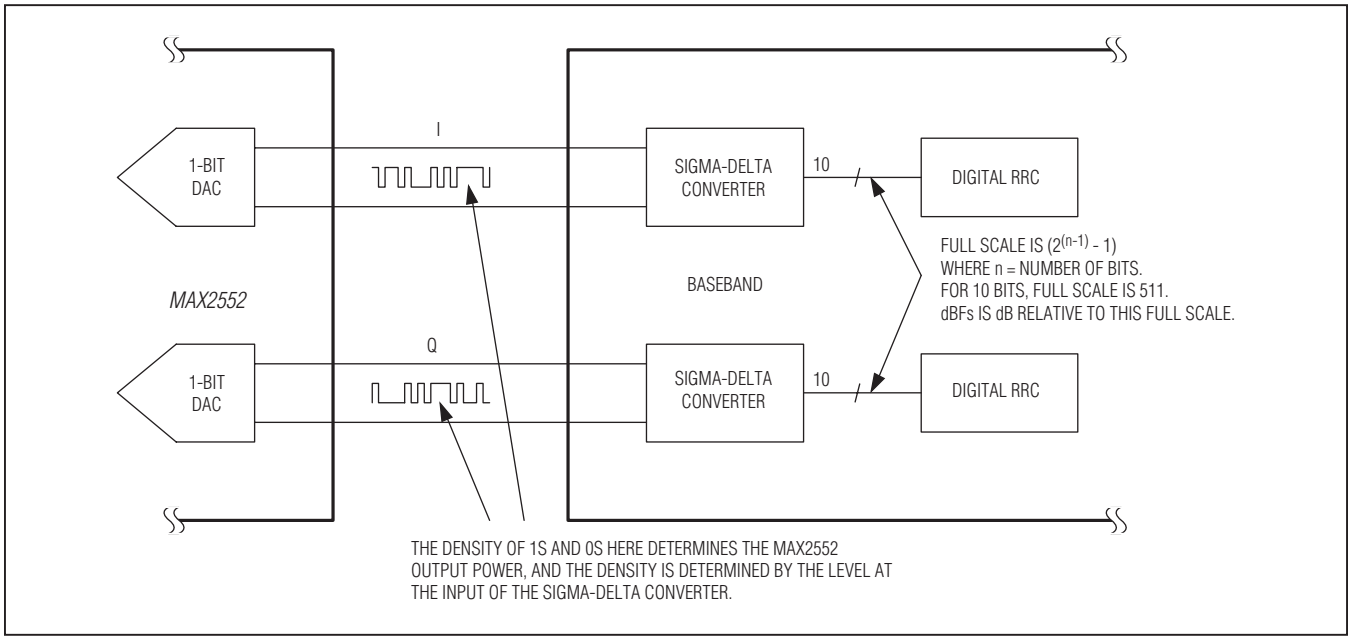


Figure 2. Baseband Input Example

RF Synthesizers

For the receiver, the RF LO frequency is programmed by the RXLO_FRAC [19:0] (fractional) register and the RXLO_SYN[7:0] (integer) register. The synthesizer frequency is demonstrated by the following example.

Assume:

$$f_{REFIN} = f_{COMPARISON} = 19.2MHz$$

$$f_{LO} = f_{REFIN} \times \left(RXLO\_SYN + \frac{RXLO\_FRAC}{2^{20}} \right) \times K$$

where:

K = 1 if RXIN1, RXIN2, RXIN5

K = 0.5 if RXIN3, RXIN4

For the transmitter, the RF LO frequency is programmed by the TXLO_FRAC [19:0] (fractional) register and the TXLO_SYN[7:0] (integer) register. The synthesizer frequency is demonstrated by the following example.

Assume:

$$f_{REFIN} = f_{COMPARISON} = 19.2MHz$$

$$f_{LO} = f_{REFIN} \times \left(TXLO\_SYN + \frac{TXLO\_FRAC}{2^{20}} \right) \times K$$

where:

K = 0.5 for TXOUTL

K = 1 for TXOUTH

Calculate the required divider ratio by dividing the LO frequency by the reference frequency.

$$Divider = \frac{f_{LO} \times 2}{f_{COMPARISON}} = \frac{1910MHz}{19.2MHz} = 99.479166$$

The integer-N divider is equal to the integer portion of the divider ratio, 99 in this example. Convert the integer-N decimal value to binary and program into the RXLO_SYN bits.

Integer-N divider = 99 = 0x63 = 0110 0011 → RXLO_SYN = 0110 0011

The fractional-N divider is equal to the fractional portion of the divider ration, 0.479166 in this example. Convert the fractional portion of the divider to a 20-bit word by multiplying by 2^{20} and rounding to the nearest whole number. Then, convert the result to binary and program the bits into the RXLO_FRAC.

Fractional-N divider = 0.479166 x 2^{20} = 502442 = 0x7AAAA → RXLO_FRAC = 0x7AAAA

ADC Clock Synthesizer

The sampling clock frequency is controlled by the CINT (BBCLK_SYN[7:0]) and CFRAC (BBCLK_FRAC[19:0]) registers. The sampling clock synthesizer does not need to be repeatedly programmed during normal operation. The sampling clock frequency (f_{ADCCLK}) is 153.6MHz in WCDMA mode and 26MHz in GSM mode. The dynamic range of the converters with this sampling frequency is sufficient to meet all system specifications with very minimal control of the PGA.

Assume:

$$f_{REFIN} = f_{COMPARISON} = 19.2MHz$$

ADC Clock Synthesizer Fractional Frequency Correction

The ADC clock synthesizer uses a 20-bit frequency synthesizer and can be enhanced by a fractional error correction. Parameters PBYQ_RATUP and PBYQ_RATDN implement the following function.

$f_{ADCCLK} = f_{REFIN}$ x (CINT + (CFRAC + PBYQ_RATUP/(PBYQ_RATUP + PBYQ_RATDN))/2^{20}) x K

PBYQ_RATUP/(PBYQ_RATUP + PBYQ_RATDN) = (f_{ADCCLK}/f_{REFIN} - CINT) x 2^{20} x K - CFRAC

where:

K = 8 if WCDMA

K = 48 if GSM/PCS/DCS

PBYQ_RATUP and PBYQ_RATDN should be chosen for the best fit.

This feature can be enabled or disabled through

EN_PBYQDIV (REG15<22>). Table 8 shows the PBYQ_RATUP and PBYQ_RATDN with commonly used crystal oscillator frequencies.

Power-Down Modes

The device features multiple power-down modes that can be controlled by hardware or software. Table 9 describes the various power-down modes.

Table 8. PBYQ_RATUP and PBYQ_RATDN Commonly Used Crystal Oscillator Frequencies

STANDARD	f_{REFIN} (MHz)	CINT REG15 <7:0>	CFRAC REG1 <19:0>	PBYQ_RATUP REG16 <7:0>	PBYQ_RATDN REG16 <15:8>	CINT REG15 <7:0>	CFRAC REG14 <19:0>	PBYQ_RATUP REG16<7:0>	PBYQ_RATDN REG16<15:8>
	REFERENCE FREQUENCY	INTEGER DIVIDE RATION (dec)	FRACTIONAL DIVIDE RATIO (dec)	FRACTIONAL LSB DITHER UP (dec)	FRACTIONAL LSB DITHER DOWN (dec)	INTEGER DIVIDE RATIO (hex)	FRACTIONAL DIVIDE RATIO (hex)	FRACTIONAL LSB DITHER UP (hex)	FRACTIONAL LSB DITHER DOWN (hex)
WCDMA	13	94	548485	59	6	5E	85E85	3B	6
	15.36	80	0	0	0	50	0	0	0
	19.2	64	0	0	0	40	0	0	0
	20	61	461373	11	14	3D	70A3D	B	E
	26	47	274242	62	3	2F	42F42	3E	3
GSM	13	96	0	0	0	60	0	0	0
	15.36	81	262144	0	0	51	40000	0	0
	19.2	65	0	0	0	41	0	0	0
	20	62	419430	2	3	3E	66666	2	3
	26	48	0	0	0	30	0	0	0

Table 9. Power-Down Modes

OPERATING MODE	REFEN PIN, REG29<14:12>	BLOCKS ENABLE REG00<18:0>	BIAS ENABLE REG20<24>	AFCDAC ENABLE REG30<19>	CDR DIVIDER ENABLE REG16<20>	CDR ENABLE REG24<18>
Sleep	0000	00000	0	0	0	0
AFC Only	0000	00000	0	1	0	0
Reference Buffer Only	1xxx or 0100	00000	0	1	0	0
Idle RX	1xxx or 0x11	00840	1	1	0	0
Idle TX	1xxx or 0x11	01000	1	1	1	1
RXIN1/TXOUTH Full Duplex	1xxx or 0x11	79BFF	1	1	1	1
RXIN1 Only	1xxx or 0x11	009FF	1	1	0	0
RXIN4 Monitor	1xxx or 0x11	009FF	1	1	0	0
RXIN5 Monitor	1xxx or 0x11	009FF	1	1	0	0
TXOUTH Only	1xxx or 0x11	79240	1	1	1	1
RXIN2	1xx or 0x11	009FF	1	1	0	0

Carrier and Sideband Suppression Optimization

The device delivers a typical carrier suppression of -40dBc and a sideband suppression of -45dBc without any external calibration; however, if greater suppression is required, the device is capable of overriding the factory settings and accepting manual calibration from the baseband processor.

RF Band Configuration

The device has configurable VCO and LO generation to support Bands III, IV, IX, and X forward and reverse link operation. In transmit signal path, LC tank is also configurable to optimize performance in both bands. Table 10 shows the key difference in SPI settings.

General-Purpose Outputs

The device is equipped with three general-purpose outputs. GPO3 can also be configured as a PLL lock detect for the Rx, Tx, or Rx and Tx. See Table 20 for how to properly configure the general-purpose outputs.

Table 10. RF Band Configuration

INPUT PIN	RF RANGE (MHz)	VCO SELECT REG03<20:19>	VCO ROH BAND REG03<22:21>	VCO DIVIDER REG03<18:17>	LNA/MIXER SELECT REG01<5:0>	RXIN4_HB REG06<16>
RXIN1	1710 to 1785	01	00	10	18	X
RXIN4 (Band V)	865 to 894	01	00	01	15	0
RXIN5	2110 to 2170	11	00	10	2A	X
RXIN2	1805 to 1880	10	11	10	1C	X

OUTPUT PIN	RF RANGE (MHz)	VCO SELECT REG28 <15:14>	VCO ROH BAND REG28 <17:16>	VCO DIVIDER REG28 <13:12>	PAD_ BAND REG19 <1:0>	PAD_ CTUNE REG19 <6:2>	TXLO_ IQ_GAIN REG20 <19>	UCX_ CSW REG21 <5:2>	T_UCX_ RSW REG22 <20:17>	T_UCX_ BAND_SEL REG22 <23:22>
TX_OUTH	1805 to 1880	10	11	10	11	00000	0	0000	0101	11
TX_OUTH	2110 to 2170	11	00	10	11	00000	0	0000	0101	11

MICROWIRE is a tradmark of National Semiconductor Corp.

Power-On Reset (POR)

Recommended defaults are not guaranteed upon power-up and are provided for reference only. All registers must be written with the proper values no earlier than 100µs after power-up. Figure 3 displays the time it takes for Tx/Rx PLL lock detect (GPO3) to become active after power-up and enabling the correct registers for proper operation. All reserved registers should only be written with default values.

Temperature Sensor

An on-chip temperature sensor is enabled by programming RX_ENABLE<14> = 1. To trigger temperature sensor ADC reading, program RX_MISC2<6> from 0 to 1. The ADC acquires the 5-bit logic output in 2µs; the temperature sensor needs to be on (RX_ENABLE<14> = 1) to maintain the ADC logic output. To read the 5-bit logic output through the DOUT pin, apply 4-wire SPI readout programming sequence to RX_MISC2<11:7>.

4-Wire Serial Interface

The device includes 32 programmable 26-bit registers. The most significant bit (MSB) is the read/write selection bit (R/W in Figure 4). The next 5 bits are register address (A[4:0] in Figure 4). The 26 least significant bits (LSBs) are register data (D[25:0] in Figure 4). Register data is loaded through the 4-wire SPI/MICROWIRE™-compatible serial interface. MSB of data at the DIN pin is shifted in first and is framed by $\overline{CS}$. When $\overline{CS}$ is low, input data is shifted at the rising edge of the clock at the SCLK pin. At $\overline{CS}$ rising edge, the 26-bit data bits are latched into the register selected by the address bits. See Figure 4. There is no power-on SPI register self-reset functionality in the device; the user must program all register values after power-up. During the read mode, register data selected by address bits is shifted out to the DOUT pin at the falling edges of the clock.

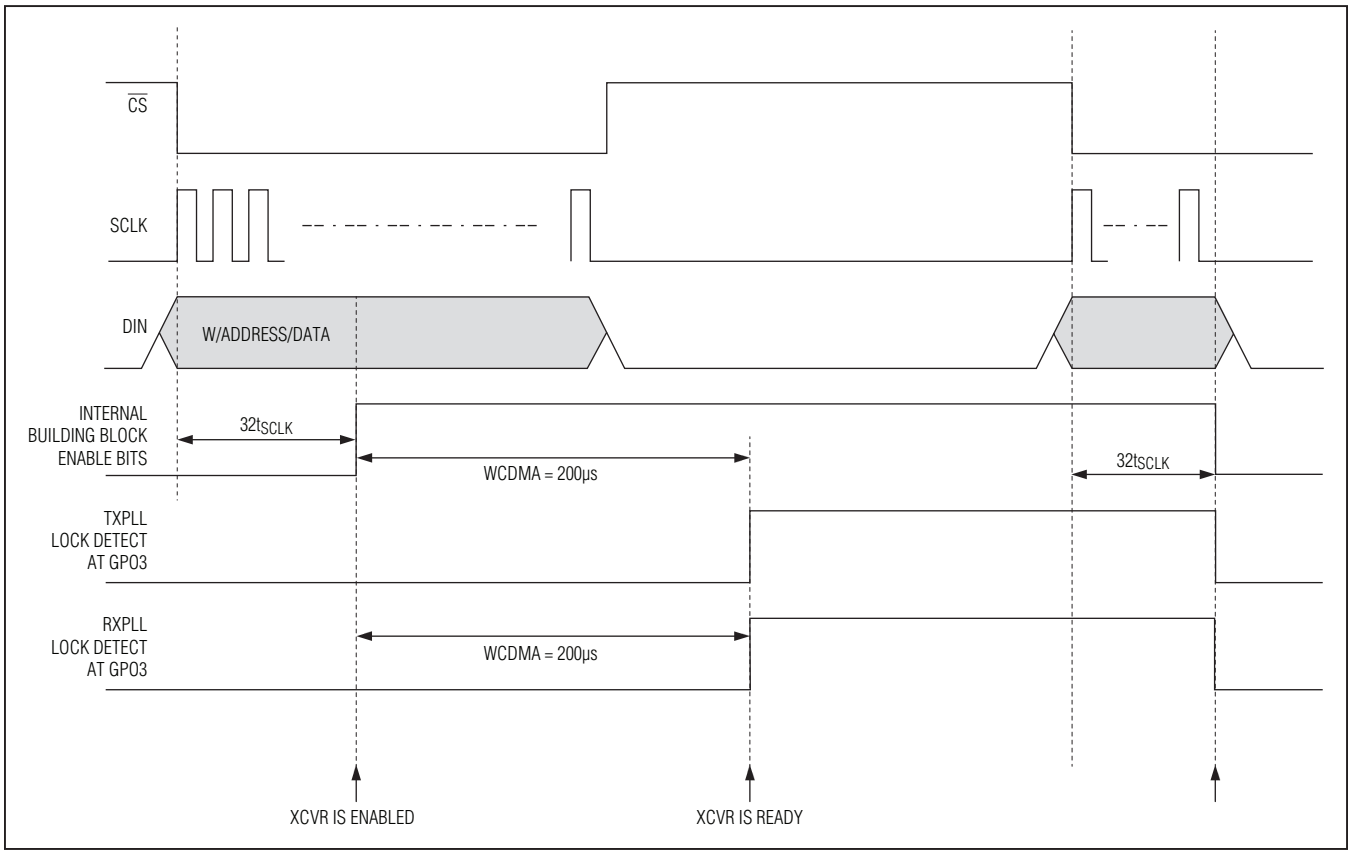


Figure 3. POR PLL Lock-Detect Time

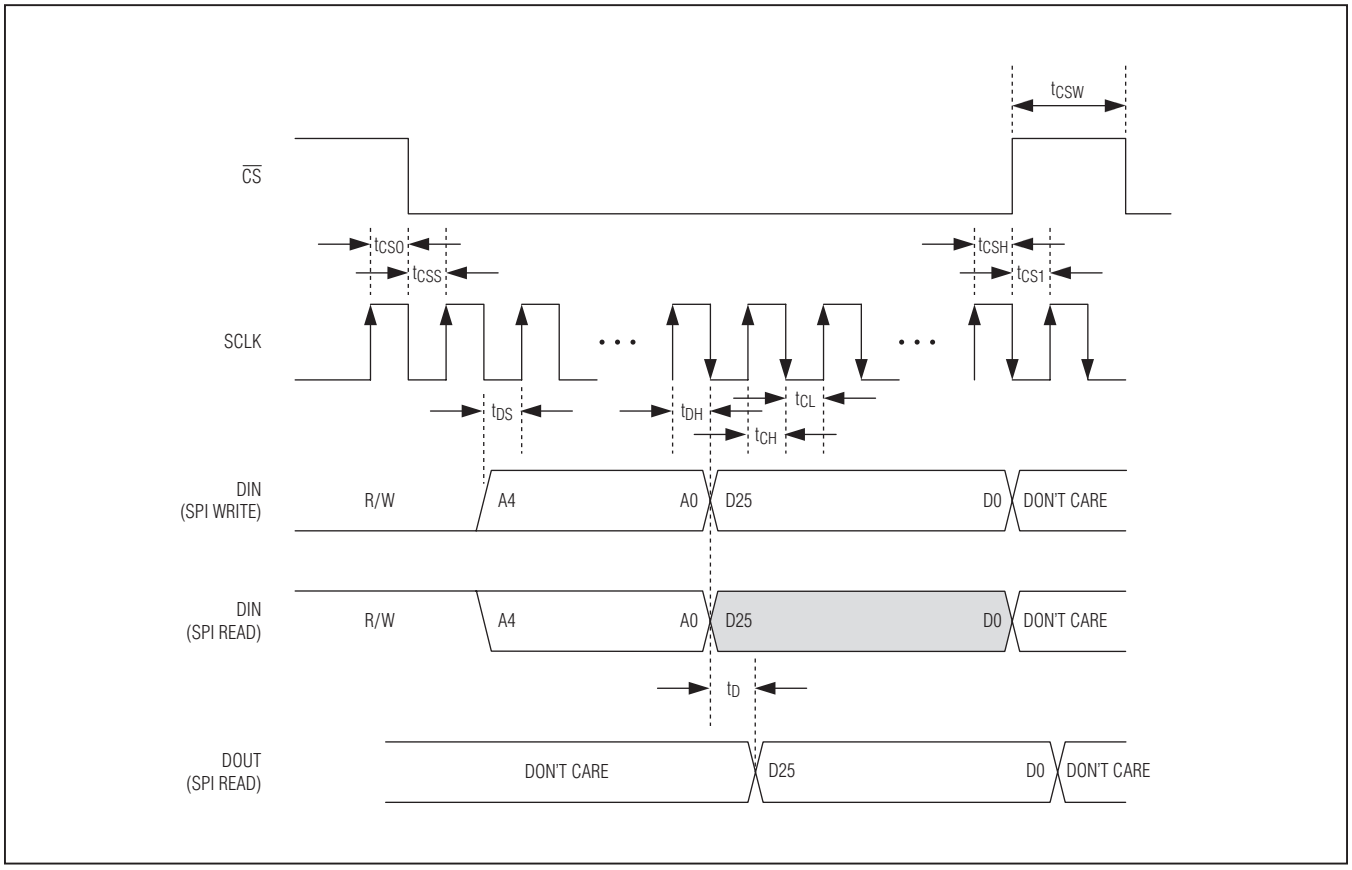


Figure 4. SPI Timing

Table 11. SPI Serial Interface Timing

SPEC NO.	PARAMETER	SYMBOL	TYP	UNITS
SPI1	SCLK Rising Edge to $\overline{CS}$ Falling Edge Wait Time	t_{CSO}	6	ns
SPI2	Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time	t_{CSS}	6	ns
SPI3	DIN to SCLK Setup Time	t_{DS}	6	ns
SPI4	DIN to SCLK Hold Time	t_{DH}	6	ns
SPI5	SCLK Pulse-Width High	t_{CH}	6	ns
SPI6	SCLK Pulse-Width Low	t_{CL}	6	ns
SPI7	Last Rising Edge of SCLK to Rising Edge of $\overline{CS}$	t_{CSH}	6	ns
SPI8	$\overline{CS}$ High Pulse Width	t_{CSW}	50	ns
SPI9	Time Between Rising Edge of $\overline{CS}$ and the Next Rising Edge of SCLK	t_{CS1}	6	ns
SPI10	SCLK Frequency	f_{CLK}	40	MHz
SPI11	Rise Time	t_R	2.5	ns
SPI12	Fall Time	t_F	2.5	ns
SPI13	SCLK Falling Edge to Valid DOUT	t_D	12.5	ns

Register and Bit Descriptions (If Applicable)

The operating mode of the device is completely controlled by 32 on-chip registers.

Recommended defaults are not guaranteed upon power-up and are provided for reference only. All registers must be written with the proper values no earlier than 10µs after power-up (once $V_{CC\_}$ is 90% of final value). All reserved registers should only be written with default values.

Table 12. Brief Register Map

REGISTER NO.	REGISTER NAME	ADDRESS	FUNCTION
0	RX_ENABLE	00000	Enable bits for various internal functions
1	RX_GAIN	00001	Gain control of LNA and PGA
2	Reserved	00010	—
3	RX_LNA	00011	LNA bias, Rx synthesizer configuration
4	Reserved	00100	—
5	Reserved	00101	—
6	RX_LPF	00110	RXLPF configuration
7	GPO_CONFIG	00111	Configuration of GPOs
8	Reserved	01000	—
9	Reserved	01001	—
10	RXLO_FRAC	01010	Receive synthesizer fractional division ratio
11	RXLO_SYN	01011	Configuration of Rx synthesizer
12	BBCLK_OUT	01100	ADC configuration
13	Reserved	01101	—
14	BBCLK_FRAC	01110	ADC clock generator fractional division ratio
15	BBCLK_SYN	01111	Configuration of clock generator synthesizer
16	BBCLK_MISC	10000	Dithering clock generator synthesizer
17	BBCLK_SPARE	10001	Miscellaneous setting for clock generator
18	TX_LPF	10010	LPF settings for Tx path
19	TX_PAD	10011	PA driver settings
20	TX_UPX1	10100	Tx upconverter bias
21	TX_UPX2	10101	Tx upconverter bias adjustment and V2I attenuation
22	TX_UPX3	10110	Tx upconverter DC offset adjustment
23	TX_GAIN1	10111	Tx path gain setting
24	TX_GAIN2	11000	Tx path gain curve adjustment
25	Reserved	11001	—
26	Reserved	11010	—
27	TXLO_FRAC	11011	Transmit synthesizer fractional division ratio
28	TXLO_SYN	11100	Configuration of Tx synthesizer
29	TXLO_REF	11101	Configuring REFOUT and REFIN
30	TXLO_AFCDAC	11110	AFC DAC word
31	Reserved	11111	—

Table 13. RX_ENABLE Register 0 (Address = 00000)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	LNAEN	LNA Enable	0 = Disable 1 = Enable	0	1	1	1	1	1	0	0	1	1	0	0	0	0	0
1	RXMXREN	Rx Mixer Enable	0 = Disable 1 = Enable	0	1	1	1	1	1	0	0	1	1	0	0	0	0	0
2	RXLPFEN	Rx LPF Enable	0 = Disable 1 = Enable	0	1	1	1	1	1	0	0	1	1	0	0	0	0	0
3	PGAQEN	Rx Q PGA Enable	0 = Disable 1 = Enable	0	1	1	1	1	1	0	0	1	1	0	0	0	0	0
4	PGAIEN	Rx I PGA Enable	0 = Disable 1 = Enable	0	1	1	1	1	1	0	0	1	1	0	0	0	0	0
5	ADCEN	ADC Enable	0 = Disable 1 = Enable	0	1	1	1	1	1	0	0	1	1	0	0	0	0	0
6	ADCCLKEN	ADC Clock Enable	0 = Disable 1 = Enable	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0
7	LVDSQ	Rx Q LVDS Enable	0 = Disable 1 = Enable	0	1	1	1	1	1	0	0	1	1	0	0	0	0	0
8	LVDSI	Rx I LVDS Enable	0 = Disable 1 = Enable	0	1	1	1	1	1	0	0	1	1	0	0	0	0	0
9	TXVGCEN	Tx VGC Enable	0 = Disable 1 = Enable	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0

Table 13. RX_ENABLE Register 0 (Address = 00000) (continued)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
10	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	RXSYNEN	Rx SYN Enable	0 = Disable 1 = Enable	0	1	1	1	1	1	0	0	1	1	1	0	0	0	0
12	TXSYNEN	Tx SYN Enable	0 = Disable 1 = Enable	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0
13	BBLBEN	BB Loopback Enable	0 = Disable 1 = Enable	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	TSEN	Temperature Sensor Enable	0 = Disable 1 = Enable	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	PADEN	PA Driver Enable	0 = Disable 1 = Enable	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0
16	TXLPFEN	Tx LPF Enable	0 = Disable 1 = Enable	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0
17	TXLOEN	Tx LO Enable	0 = Disable 1 = Enable	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0
18	UPCXEN	Upconverter Enable	0 = Disable 1 = Enable	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0

Table 13. RX_ENABLE Register 0 (Address = 00000) (continued)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
19	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 14. RX_GAIN Register 1 (Address = 00001)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	LNASEL [2:0]	LNA Selection	<2:0> = 000 = RXIN1 <2:0> = 100 = RXIN2 <2:0> = 001 = RXIN3 <2:0> = 101 = RXIN4 <2:0> = X10 = RXIN5	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
2				2	0	1	1	1	0	0	0	0	0	0	0	0	0	0
3	BandSel_Mix	Rx Mixer Select	0 = CEL mixer (default) 1 = PCS mixer	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1
4	MX_SW [1:0]	Rx Mixer Input Select	If BandSel_Mix = 1 (PCS) 00 = DCS input 01 = PCS input 10 = IMT input 11 = None	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1
5			If BandSel_Mix = 0 (CELL) 11 = None X0 = CELL input X1 = GSM input	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
6	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	PGAGAIN [3:0]	Rx PGA Gain Control	<3:0> = 0000 = Min gain (default) <3:0> = 0001 = Min gain + 3dB … <3:0> = 1110 = Max gain - 3dB <3:0> = 1111 = Max gain	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
9				1	1	0	0	1	1	0	0	1	1	1	0	0	0	0
10				2	1	1	1	0	0	0	0	1	1	1	0	0	0	0
11				3	0	1	1	1	1	0	0	0	0	0	0	0	0	0

Table 14. RX_GAIN Register 1 (Address = 00001) (continued)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
12	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	LNAGAIN[1:0]	LNA Gain Control	<1:0> = 00 = Low gain <1:0> = 01 = Mid gain (not available for RXIN4) <1:0> = 10 = High gain (default) <1:0> = 11 = Do **not** use	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				9	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15. Reserved Register 2 (Address = 00010)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19				19	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				20	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				21	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				22	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				23	1	1	1	1	1	1	1	1	1	1	1	1	1	1
24				24	1	1	1	1	1	1	1	1	1	1	1	1	1	1
25				25	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 16. RX_LNA Register 3 (Address = 00011)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	1	1	1	1	1	1	1	1	1	1	1	1	1	1
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	1	1	1	1	1	1	1	1	1	1	1	1	1	1
8				8	1	1	1	1	1	1	1	1	1	1	1	1	1	1
9				9	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	RXSYN_RBYP	Rx SYN Ena Rx RF oop Filter ble	Rx RF PLL Loop Filter Adjust 0 = WCDMA 1 = Not used	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	Reserved	Reserved	—	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				3	1	1	1	1	1	1	1	1	1	1	1	1	1	1
15				4	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16				5	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 16. RX_LNA Register 3 (Address = 00011) (continued)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
17	RVCO_DIV2 [1:0]		Rx RF VCO Prescaler Divide Ratio Configuration [1:0] = 01 = CELL [1:0] = 10 = PCS	6	0	0	0	1	0	0	0	0	0	0	0	0	0	0
18				7	1	1	1	0	1	1	1	1	1	1	1	1	1	1
19	RVCO_SEL [1:0]	Rx RF VCO Selection	[1:0] = 00 = Disable [1:0] = 01 = ROL (CELL) [1:0] = 10 = ROH (PCS) [1:0] = 11 = Not used	8	1	0	0	1	1	1	1	1	1	1	1	1	1	1
20				9	0	1	1	0	1	0	0	0	0	0	0	0	0	0
21	RVCOTUNE [1:0]	Rx RF VCO ROH Band Selection	[1:0] = 00 = band2 (IMT) [1:0] = 01 = band3 (PCS) [1:0] = 11 = Not used	10	0	0	1	0	0	0	0	0	0	0	0	0	0	0
22				0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
23	Reserved	Reserved	—	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
24				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17. Reserved Register 4 (Address = 00100)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	1	1	1	1	1	1	1	1	1	1	1	1	1	1
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12				12	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	1	1	1	1	1	1	1	1	1	1	1	1	1	1
18				18	1	1	1	1	1	1	1	1	1	1	1	1	1	1
19				19	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				20	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				21	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				22	1	1	1	1	1	1	1	1	1	1	1	1	1	1
23				23	1	1	1	1	1	1	1	1	1	1	1	1	1	1
24				24	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				25	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 18. Reserved Register 5 (Address = 00101)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7				7	1	1	1	1	1	1	1	1	1	1	1	1	1	1
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	1	1	1	1	1	1	1	1	1	1	1	1	1	1
15				15	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				16	1	1	1	1	1	1	1	1	1	1	1	1	1	1
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	1	1	1	1	1	1	1	1	1	1	1	1	1	1
19				19	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				20	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				21	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				22	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				23	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				24	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				25	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 19. RX_LPF Register 6 (Address = 00110)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	1	1	1	1	1	1	1	1	1	1	1	1	1	1
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	1	1	1	1	1	1	1	1	1	1	1	1	1	1
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	1	1	1	1	1	1	1	1	1	1	1	1	1	1
11				11	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12				12	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13				13	1	1	1	1	1	1	1	1	1	1	1	1	1	1
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17	LPFBYPASS	Rx LPF Bypass	0 = Normal operation 1 = Bypass Rx LPF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23	BBMODE	Rx LPF Bandwidth Select	000 = WCDMA 011 = GSM	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
24				1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
25				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 20. GPO_CONFIG Register 7 (Address = 00111)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	GPO3_LD_RD_sel_LSB		GPO3 Output Mux Select LSB MSB in REG7<17> 00 = RXPLL LD 01 = TXPLL LD 10 = Output selected by GPO3<1:0> 11 = RXPLL LD and TXPLL LD and CLKPLL LD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	GPO2<1:0>	GPO2 GPO2 Output Select Select	<1:0> = 00 = High-Z <1:0> = 01 = High-Z <1:0> = 10 = Low-Z low <1:0> = 11 = Low-Z high	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
3				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	GPO3<1:0>	GPO3 Output Select	<1:0> = 00 = High-Z <1:0> = 01 = High-Z <1:0> = 10 = Low-Z low <1:0> = 11 = Low-Z high	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
5				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	TS_TRIG	Temperature Sensor Reading Trigger	0 = Not trigger reading 1 = Trigger reading	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 20. GPO_CONFIG Register 7 (Address = 00111) (continued)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
7		Temperature Sensor Output	To be read at DOUT pin through SPI readback	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
15				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				4	1	1	1	1	1	1	1	1	1	1	1	1	1	1
17	GPO3_LD_RD_sel_MSB		GPO3 Output Mux Select MSB LSB in REG7<1> 00 = RXPLL LD 01 = TXPLL LD 10 = Output selected by GPO3<0:1> 11 = RXPLL LD and TXPLL LD and CLKPLL LD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
19				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
20	DOUT_DRV <1:0>	DOUT Drive Strength	<1:0> = 00 = 1x <1:0> = 01 = 2x <1:0> = 10 = 3x <1:0> = 11 = 4x	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
21				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
22	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 21. Reserved Register 8 (Address = 01000)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19				19	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				20	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				21	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				22	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				23	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				24	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				25	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 22. Reserved Register 9 (Address = 01001)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19				19	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				20	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				21	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				22	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				23	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				24	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				25	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 23. RXLO_FRAC Register 10 (Address = 01010)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	RFFRAC [19:0]	Receiver RF Synthesizer Fractional Division Ratio	See the *RF Synthesizers* section	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
1				1	0	1	0	1	0	1	0	0	1	0	0	0	0	0
2				2	0	0	1	0	1	0	0	0	0	0	0	0	0	0
3				3	0	1	0	1	0	1	0	0	1	0	0	0	0	0
4				4	0	0	1	0	1	0	0	0	0	0	0	0	0	0
5				5	0	1	0	1	0	1	0	0	1	0	0	0	0	0
6				6	0	0	1	0	1	0	0	0	0	0	0	0	0	0
7				7	0	1	0	1	0	1	0	0	1	0	0	0	0	0
8				8	0	0	1	0	1	0	0	0	0	0	0	0	0	0
9				9	0	1	0	1	0	1	0	0	1	0	0	0	0	0
10				10	0	0	1	0	1	0	0	0	0	0	0	0	0	0
11				11	0	1	0	1	0	1	0	0	1	0	0	0	0	0
12				12	0	0	1	0	1	0	0	0	0	0	0	0	0	0
13				13	0	1	0	1	0	1	0	0	1	0	0	0	0	0
14				14	1	1	0	0	0	1	1	1	1	1	1	1	1	1
15				15	1	0	0	1	0	1	1	1	1	1	1	1	1	1
16				16	1	1	0	0	1	0	1	1	0	1	1	1	1	1
17				17	1	1	0	1	0	0	1	1	0	1	1	1	1	1
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19				19	0	0	0	1	0	0	0	0	0	0	0	0	0	0
20	Reserved	—	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
21				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				5	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 24. RXLO_SYN Register 11 (Address = 01011)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	RINT[7:0]	Rx RF PLL Integer Divide Ratio	See the *RF Synthesizers* section	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0
1				0	1	1	0	1	1	0	1	1	0	1	1	1	1	1
2				0	0	1	0	0	1	1	0	0	1	0	0	0	0	0
3				0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
4				0	1	0	0	1	0	1	1	1	1	1	1	1	1	1
5				0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
6				0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	RRD	Rx Reference Divide Ratio	0 = Divide-by-1 1 = Divide-by-2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10				0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
11				0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	RCPI[2:0]	Rx PLL Charge-Pump Current	Rx RF PLL Charge-Pump Current 000 = Not used 001 = 200µA 011 = 600µA 110 = 1200µA	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
19				0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
20				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21	Reserved	Reserved	—	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				4	1	1	1	1	1	1	1	1	1	1	1	1	1	1
24				5	1	1	1	1	1	1	1	1	1	1	1	1	1	1
25				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 25. BBCLK_OUT Register 12 (Address = 01100)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	ADF[2:0]	ADC Clock Divide Ratio	000 = 1 for WCDMA 001 = Not used 010 = Not used 011 = 6 for GSM 100~111 = Not used	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	LVDSI_2X	RxBB LVDS 2X Current Enable	0 = 220Ω load 1 = 100Ω load	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
11				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19				9	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				10	1	1	1	1	1	1	1	1	1	1	1	1	1	1
21				11	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				12	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				14	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				15	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 26. Reserved Register 13 (Address = 01101)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2				0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
3				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				3	1	1	1	1	1	1	1	1	1	1	1	1	1	1
6				0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				5	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12				0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13				0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
14				0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
15				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
18				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
19				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 27. BBCLK_FRAC Register 14 (Address = 01110)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	CFRAC [19:0]	ADC Clock PLL Fractional Divide Ratio	WCDMA: For f_{REFIN} = 13.0MHz = 85E85 (hex) 15.36MHz = 00000 (hex) 19.2MHz = 00000 (hex) 26.0MHz = 42F4s (hex) GSM: For f_{REFIN} = 13.0MHz = 00000 (hex) 15.36MHz = 40000 (hex) 19.2MHz = 00000 (hex) 26.0MHz = 00000 (hex)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19				19	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
21				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 28. BBCLK SYN Register 15 (Address = 01111)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	CINT[7:0]	ADC Clock PLL Integer Divide Ratio	GSM: For f_{REFIN} = 13.0MHz = 60 (hex) 15.36MHz = 51 (hex) 19.2MHz = 41 (hex) 26.0MHz = 30 (hex) WCDMA: For f_{REFIN} = 13.0MHz = 5E (hex) 15.36MHz = 50 (hex) 19.2MHz = 40 (hex) 26.0MHz = 2F (hex)	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	CRD	ADC Clock PLL Reference Divide Ratio	0 = Divide-by-1 (default) 1 = Divide-by-2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
11				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 28. BBCLK SYN Register 15 (Address = 01111) (continued)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
18	CCPI[2:0]	ADC Clock PLL Charge Pump Current	000 = 0µA, do **not** use 001 = 25µA 010 = 50µA (f_{REFIN} = 26MHz) 011 = 75µA (f_{REFIN} = 19.2MHz 100 = 100µA (f_{REFIN} = 13MHz) 111 = 175µA	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
19				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
20				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22	EN_PBYQDIV	ADC Clock PLL P/Q Rational Division Enable	ADC Clock PLL P/Q Rational Division Enable 0 = Disabled 1 = Enable	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
23	CINTB	ADC Clock PLL Integer/ Fractional Mode	ADC Clock Integer/Fractional Mode 0 = Integer mode 1 = Fractional mode	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
24	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 29. BBCLK_MISC Register 16 (Address = 10000)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	PBYQ_RATUP[7:0]	ADC Clock Fractional LSB Dither **Up** Number of Cycles LSB Is High	WCDMA: For f_{REFIN} = 13.0MHz = 3B (hex) 15.36MHz = 00 (hex) 19.2MHz = 00 (hex) 20.0MHz = 0B (hex) 26.0MHz = 3E (hex) GSM: For f_{REFIN} = 13.0MHz = 00 (hex) 15.36MHz = 00 (hex) 19.2MHz = 00 (hex) 26.0MHz = 00 (hex)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	PBYQ_RATDN[7:0]	ADC Clock Fractional LSB Dither **Down** Number of Cycles LSB Is Low	DC Clock Fractional LSB Dither **Down**. Number of cycles LSB is low. WCDMA: For f_{REFIN} = 13.0MHz = 06 (hex) 15.36MHz = 00 (hex) 19.2MHz = 00 (hex) 20.0MHz = 0E (hex) 26.0MHz = 03 (hex) GSM: For f_{REFIN} = 13.0MHz = 00 (hex) 15.36MHz = 00 (hex) 19.2MHz = 00 (hex) 26.0MHz = 00 (hex)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 29. BBCLK_MISC Register 16 (Address = 10000) (continued)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
16	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
19				3	1	1	1	1	1	1	1	1	1	1	1	1	1	1
20	CDR_DIV2_EN	CLK VCO to CDR Divide-by-2 Enable	CLK VCO to CDR Divide-by-2 Enable 0 = Disable 1 = Enable	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0
21	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 30. BBCLK_SPARE Register 17 (Address = 10001)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12				12	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	DIE_ID_sel	Die ID Readout Select	Affect REG17[25:19] 0 = Read register value 1 = Read die ID	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19	DIE_ID[6:0]	Die ID Readout Bits at DOUT pin	DIE_ID[2:0] 001 = 1Z 010 = 2Z 011 = 3Z	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 31. TX_LPF Register 18 (Address = 10010)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	TXLPFB [2:0]	TXLPF Bandwidth	000 = Do not use 001 = WCDMA 010 = Do not use 011 = Do not use 100~111 = Do not use	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
6				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	TXLPFMD [1:0]	TXLPF Operating Mode	[1:0] = 00 = Shut down [1:0] = 01 = LPF bypass [1:0] = 10 = Do not use [1:0] = 11 = Normal operation (WCDMA	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
9				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	BBLB	TXLPF Baseband Loopback	0 = Enable loopback 1 = Normal operation	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 31. TX_LPF Register 18 (Address = 10010) (continued)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
11	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
14				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				4	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16				5	1	1	1	1	1	1	1	1	1	1	1	1	1	1
17				6	1	1	1	1	1	1	1	1	1	1	1	1	1	1
18				7	1	1	1	1	1	1	1	1	1	1	1	1	1	1
19				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				9	1	1	1	1	1	1	1	1	1	1	1	1	1	1
21				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				11	1	1	1	1	1	1	1	1	1	1	1	1	1	1
23				12	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25	TXINDACF	Tx DAC Bandwidth Select	Tx DAC Bandwidth 1 = 15MHz	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 32. TX_PAD Register 19 (Address = 10011)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	PAD_BAND [2:0]	PA Driver Frequency Band	[1:0] = 00 = CELL [1:0] = 01 = Do not use [1:0] = 10 = PCS [1:0] = 11 = Do not use	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	PAD_CTUNE [4:0]	PA Driver Center Frequency Select	CELL = 00100 PCS = 10001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10				3	1	1	1	1	1	1	1	1	1	1	1	1	1	1
11				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				6	1	1	1	1	1	1	1	1	1	1	1	1	1	1
14				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				8	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16				9	1	1	1	1	1	1	1	1	1	1	1	1	1	1
17				10	1	1	1	1	1	1	1	1	1	1	1	1	1	1
18				11	1	1	1	1	1	1	1	1	1	1	1	1	1	1
19				12	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				14	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				15	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				16	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				17	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				18	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 33. TX_UPX1 Register 20 (Address = 10100)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	1	1	1	1	1	1	1	1	1	1	1	1	1	1
5				5	1	1	1	1	1	1	1	1	1	1	1	1	1	1
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	1	1	1	1	1	1	1	1	1	1	1	1	1	1
8				8	1	1	1	1	1	1	1	1	1	1	1	1	1	1
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13				13	1	1	1	1	1	1	1	1	1	1	1	1	1	1
14				14	1	1	1	1	1	1	1	1	1	1	1	1	1	1
15				15	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16				16	1	1	1	1	1	1	1	1	1	1	1	1	1	1
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19	TXLO_IQ_GAIN	TXLO IQ Phase Adjust Slope	0 = PCS bands 1 = CELL band	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
21				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24	BIAS_EN	Master Bias Enable	0 = Disable 1 = Enable	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0
25	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 34. TX_UPX2 Register 21 (Address = 10101)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	UCX_CSW[<3:0]	UCX Tank Frequency Adjust	0000 = PCS 1101 = CELL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12				6	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				9	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				11	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18				12	1	1	1	1	1	1	1	1	1	1	1	1	1	1
19				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				14	1	1	1	1	1	1	1	1	1	1	1	1	1	1
21				15	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				16	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				17	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				18	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				19	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 35. TX_UPX3 Register 22 (Address = 10110)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	1	1	1	1	1	1	1	1	1	1	1	1	1	1
6				6	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7				7	1	1	1	1	1	1	1	1	1	1	1	1	1	1
8				8	1	1	1	1	1	1	1	1	1	1	1	1	1	1
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	1	1	1	1	1	1	1	1	1	1	1	1	1	1
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19				19	1	1	1	1	1	1	1	1	1	1	1	1	1	1
20				20	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				21	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22	T_UCX_BAND_SEL [1:0]	Upconverter Band Select	[1:0] = 00 = Do not use [1:0] = 01 = CELL band [1:0] = 10 = Do not use [1:0] = 11 = PCS band	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
23				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
24	UCX_V2I_MODE_F [1:0]	Upconverter V2I Bandwidth	[1:0] = 00 = Do not use [1:0] = 01 = WCDMA [1:0] = 10 = Do not use [1:0] = 11 = Do not use	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
25				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 36. TX_GAIN1 Register 23 (Address = 10111)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	TX_GAIN [9:0]	Tx Gain	000 (hex) = Minimum gain 3FF (hex) = Maximum gain	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4				4	1	1	1	1	1	1	1	1	1	1	1	1	1	1
5				5	1	1	1	1	1	1	1	1	1	1	1	1	1	1
6				6	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7				7	1	1	1	1	1	1	1	1	1	1	1	1	1	1
8				8	1	1	1	1	1	1	1	1	1	1	1	1	1	1
9				9	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				4	1	1	1	1	1	1	1	1	1	1	1	1	1	1
15				5	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19				9	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				11	1	1	1	1	1	1	1	1	1	1	1	1	1	1
22				12	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24	GPO1[1:0]	GPO1 Output Select	[1:0]= 00 = High-Z [1:0]= 01 = High-Z [1:0]= 10 = Low-Z low [1:0]= 11 = Low-Z high	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
25				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 37. TX_GAIN2 Register 24 (Address = 11000)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	TXINDACI [5:0]	TXBB DAC Bias Current	TXBB DAC Bias Current 010100 = WCDMA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
9				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				4	1	1	1	1	1	1	1	1	1	1	1	1	1	1
11				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	TXINDACZI	TXBB Differential Input Impedance	0 = 220Ω 1 = 100Ω	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 37. TX_GAIN2 Register 24 (Address = 11000) (continued)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
13	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	CDR_EN	CDR Enable	CDR Enable 0 = Disable 1 = Enable	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0
19	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
20				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
21	TXBB_LVDS_DDR3	TXBB Input LVDS/DDR3 Select	TXBB Input LVDS/DDR3 Select 0 = LVDS 1 = DDR3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 38. Reserved Register 25 (Address = 11001)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19				19	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				20	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				21	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				22	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				23	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				24	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				25	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 39. Reserved Register 26 (Address = 11010)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7				7	1	1	1	1	1	1	1	1	1	1	1	1	1	1
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	1	1	1	1	1	1	1	1	1	1	1	1	1	1
15				15	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19				19	1	1	1	1	1	1	1	1	1	1	1	1	1	1
20				20	1	1	1	1	1	1	1	1	1	1	1	1	1	1
21				21	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				22	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				23	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				24	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				25	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 40. TXLO_FRAC Register 27 (Address = 11011)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	TFRAC [19:0]	Tx RF PLL Fractional Divide Ratio	AAAAB (hex) = CELL 36AAB (hex) = PCS	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	1	1	1	1	1	1	1	1	1	1	1	1	1	1
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	1	1	1	1	1	1	1	1	1	1	1	1	1	1
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	1	1	1	1	1	1	1	1	1	1	1	1	1	1
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				16	1	1	0	1	1	0	1	1	0	1	1	1	1	1
17				17	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18				18	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19				19	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
21				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				6	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 41. TXLO_SYN Register 28 (Address = 11100)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	TINT[7:0]	Tx RF PLL Integer Divide Ratio	5B (hex) = CELL 66 (hex) = PCS	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1				1	1	1	0	1	1	0	1	1	0	1	1	1	1	1
2				2	1	1	0	1	1	0	1	1	0	1	1	1	1	1
3				3	1	1	0	1	1	0	1	1	0	1	1	1	1	1
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	1	1	1	1	1	1	1	1	1	1	1	1	1	1
6				6	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	TRD	Tx Reference Divide Ratio	0 = Divide-by-1 1 = Divide-by-2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
11				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12	TVCO_DIV2 [1:0]	Tx RF VCO Prescaler Divide Ratio Configuration	[1:0] = 01 = CELL [1:0] = 10 = PCS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 41. TXLO_SYN Register 28 (Address = 11100) (continued)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
14	TVCO_SEL [1:0]	Tx RF VCO Selection	[1:0]= 00 = Disable [1:0]= 01 = ROL [1:0]= 10 = ROH [1:0]= 11 = Not used	0	1	1	0	1	1	0	1	1	0	1	1	1	1	1
15				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16	Reserved	Reserved	—	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0
17				1	0	0	1	0	0	1	0	0	1	0	0	0	0	0
18	TCPI<2:0>	Tx RF PLL Charge Pump Current	000 = 0µA, 001 = 200µA … 100 = 800µA … 110 = 1200µA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
21	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
22				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
24				3	1	1	1	1	1	1	1	1	1	1	1	1	1	1
25				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 42. TXLO_REF Register 29 (Address = 11101)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	1	1	1	1	1	1	1	1	1	1	1	1	1	1
9				9	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	REFIN_ENOUT1	Reference Rx PLL Output Enable	Reference for Rx PLL Enable 0 = Disable 1 = Enable	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0
13	REFIN_ENOUT2	Reference Tx PLL Output Enable	Reference for Tx PLL Enable 0 = Disable 1 = Enable	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0

Table 42. TXLO_REF Register 29 (Address = 11101) (continued)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
14	REFIN_ENOUT3	REFOUT Enable	REFOUT Enable 0 = Disable 1 = Enable	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0
15	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18				3	1	1	1	1	1	1	1	1	1	1	1	1	1	1
19				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20				5	1	1	1	1	1	1	1	1	1	1	1	1	1	1
21	REFOUT_ DRV[1:0]	REFOUT Buffer Drive Strength	REFOUT Drive Strength 00 = 1x 01 = 2x 10 = 3x 11 = 4x	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
22				1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
23	REFOUT_LV_ CMOS_SEL	REFOUT Output Driver Select	0 = CMOS 1 = Low voltage	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 43. TXLO_AFCDAC Register 30 (Address = 11110)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	AFCDAC [11:0]	AFCDAC Output Voltage	800 (hex) V_{AFCOUT} = 0.4 + (2.5 - 0.4) x AFCDAC/212	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19	AFCDAC_EN	AFCDAC Enable	0 = Disable 1 = Enable	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
20	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22				2	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 44. Reserved Register 31 (Address = 11111)

BIT	BIT ID	NAME	DEFINITION	BIT	BAND III, IV, IX, OR X, RX1 ONLY	BAND II PCS RX2 ONLY	BAND III OR IX RX2 ONLY	BAND V RX4 ONLY	BAND IV OR X RX5 ONLY	BANDS III OR IX TXH ONLY	BANDS IV OR X TXH ONLY	BANDS IV OR X RX1/TXH FDD	BANDS III OR IX RX1/TXH FDD	BAND III, IV, IX, OR X RX IDLE	BAND III, IV, IX, OR X TX IDLE	AFC ONLY	REFERENCE BUFFER	SLEEP
0	Reserved	Reserved	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1				1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2				2	1	1	1	1	1	1	1	1	1	1	1	1	1	1
3				3	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4				4	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5				5	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6				6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7				7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8				8	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9				9	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10				10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11				11	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12				12	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13				13	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14				14	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15				15	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16				16	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17				17	1	1	1	1	1	1	1	1	1	1	1	1	1	1
18				18	1	1	1	1	1	1	1	1	1	1	1	1	1	1
19				19	1	1	1	1	1	1	1	1	1	1	1	1	1	1
20				20	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21				21	1	1	1	1	1	1	1	1	1	1	1	1	1	1
22				22	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23				23	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24				24	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25				25	0	0	0	0	0	0	0	0	0	0	0	0	0	0

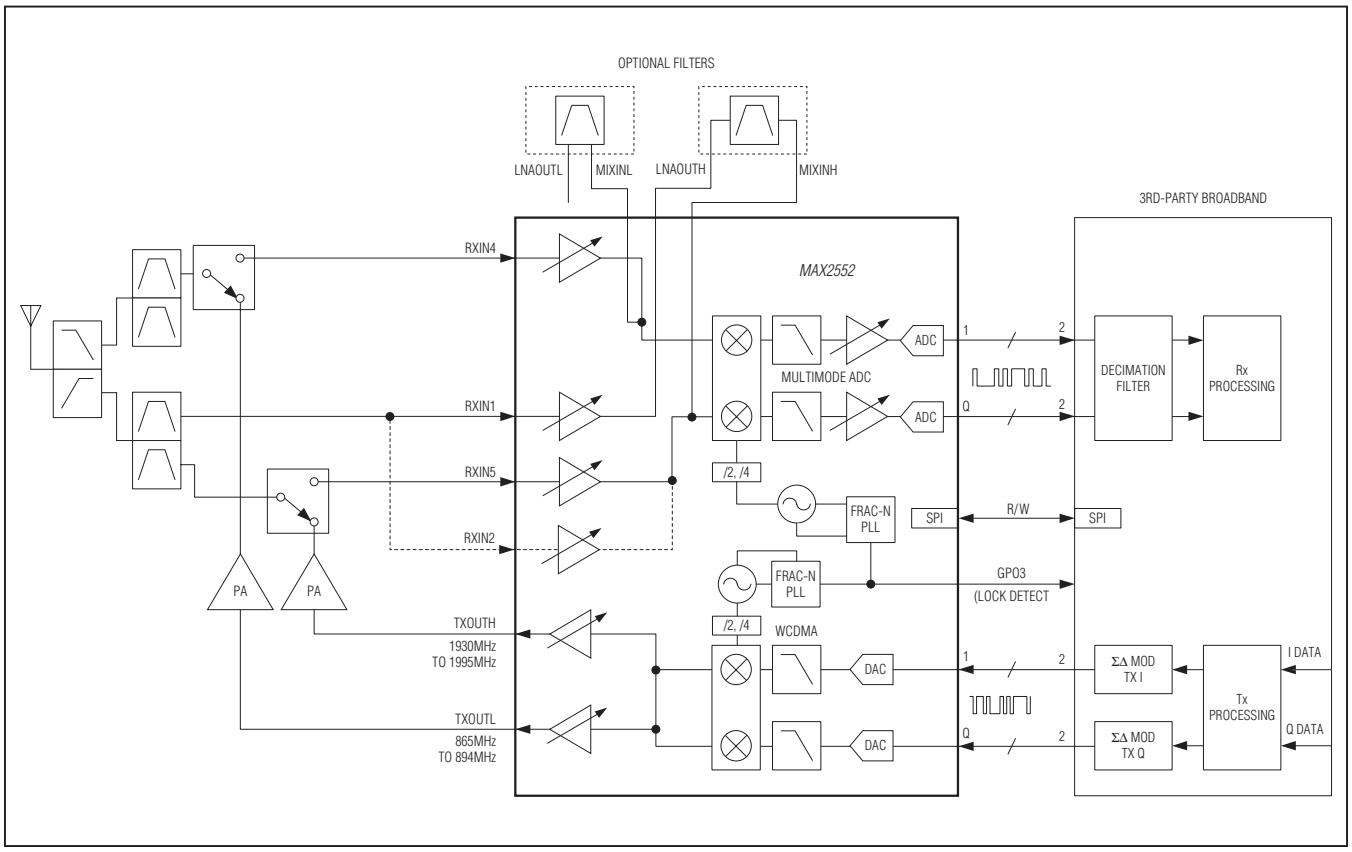
Band III, IV, IX, and X WCDMA Femtocell Transceiver with GSM Monitoring

Applications Information

Layout Considerations

The EV kit and reference design serve as a guide for PCB layout. Keep RF signal lines as short as possible to minimize losses and radiation. Use controlled impedance on all high-frequency traces. The exposed pad must be soldered evenly to the board's ground plane for proper operation. Use abundant ground vias between RF traces to minimize undesired coupling. Bypass each $V_{CC\_}$ pin to ground with capacitors placed as close as possible to the pin.

Simplified Block Diagram



Ordering Information

PART	BAND	TEMP RANGE	PIN-PACKAGE
MAX2552ETN+	III, IV, IX and X	-40°C to +85°C	56 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
56 TQFN-EP	T5677+2	21-0144	90-0043

MAX2552

Band III, IV, IX, and X WCDMA Femtocell Transceiver with GSM Monitoring

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/13	Initial release	—