

xCORE-200 sliceKIT Hardware Manual

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1 Introduction

The xCORE-200 sliceKIT (XK-SK-200-ST) contains a fully pinned out XE216-512-FB236 device, making it suitable for prototyping xCORE-200 applications. USB connectivity is on-board and the GPIOs are connected to expansion connectors (termed slots) to interface with expansion cards that plug into the slots to support any interface you require. The board contains all circuitry necessary for operating and debugging the XMOS system. Multiple sliceKIT-200 boards can be interconnected to form a multiple xCORE device system connected by high speed XMOS Links between the boards.

The kit is supplied with the following contents:

- ▶ xCORE-200 core board (XP-SKC-X200)
- ▶ xTAG Debugger (XA-XTAG)
- ▶ Debug Adapter (XA-SK-DEBUG) for interfacing the XTAG to the core board
- ▶ Gigabit Ethernet slice (XA-SK-GBE), a dual slot slice for 1000Mbps applications
- ▶ GPIO slice (XA-SK-GPIO)
- ▶ 12V wall mounted PSU

The xCORE-200 sliceKIT is also compatible with the existing 10/100Mbps Ethernet slice (XA-SK-E100), which only occupies a single slot.

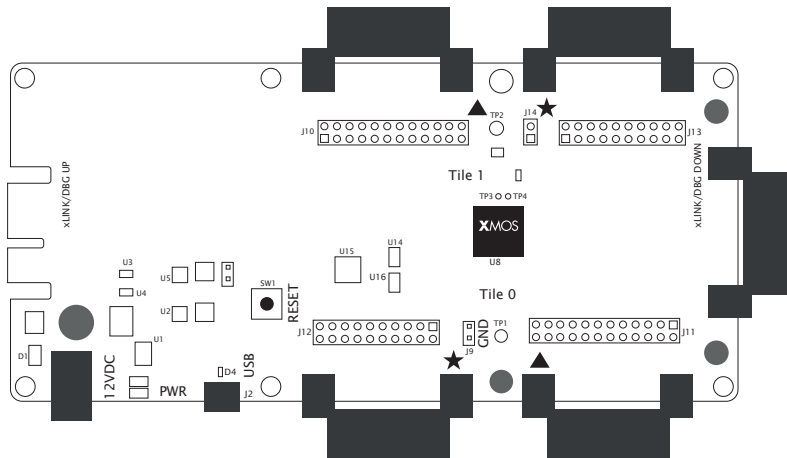


Figure 1:
xCORE-200
sliceKIT core
board block
diagram

2 xCORE Multicore Microcontroller Device

xCORE-200 sliceKIT (XK-SK-200-ST) is based on a two-tile xCORE-200 device (XE216-512-FB236). Each tile is user-programmable, providing eight logical cores with a total of up to 1000 MIPS compute. All 128 general-purpose digital I/O have been brought out to header pins, providing tremendous flexibility for a wide range of USB and networked audio products to be developed on a common platform.

For information on xCORE-200 tiles and cores see the xCORE-200 Architecture Overview¹.

3 USB

A micro-B USB connector (J2) is included on the xCORE-200 core board for USB 2.0 applications. The data signals are connected directly to the XE216 device. The core board cannot be powered from the USB VBUS supply.

4 xCORE-200 Digital I/O Sockets

All digital I/O connected to the 1/4/8/16 bit xCORE ports are brought out to four PCIe sockets; Tile 0 is connected to J3/J4 and Tile 1 connected to J6/J7. Each of the headers has an identifying symbol that is used to identify suitable sliceCARDS that fit the I/O and slot - X*n*D refers to the respective xCORE Tile 0 or 1.

The tables below show the configuration of the I/O and ports connected to each header:

¹<http://www.xmos.com/published/xcore-architecture>

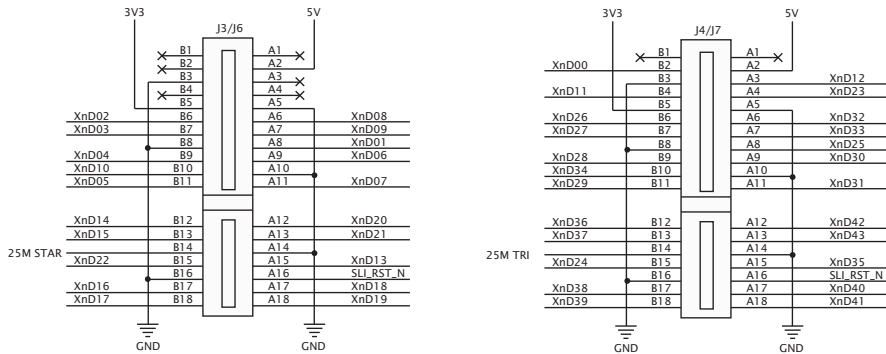


Figure 2:
xCORE-200
sliceKIT I/O
sockets

4.1 Star Socket (J3/J6)

PCIE A (BOT)	SIGNAL	FUNCTION and PORTS
A1	NC	NOT CONNECTED
A2	5V	5V
A3	NC	NOT CONNECTED
A4	NC	NOT CONNECTED
A5	GND	POWER SUPPLY GROUND
A6	XnD08	P4A2 P8A6 P16A6 P32A26
A7	XnD09	P4A3 P8A7 P16A7 P32A27
A8	XnD01	P1B0
A9	XnD06	P4B2 P8A4 P16A4 P32A24
A10	GND	POWER SUPPLY GROUND
A11	XnD07	P4B3 P8A5 P16A5 P32A25
KEY	KEY	MECHANICAL KEY
A12	XnD20	P4C2 P8B6 P16A14 P32A30
A13	XnD21	P4C3 P8B7 P16A15 P32A31
A14	GND	POWER SUPPLY GROUND
A15	XnD13	P1F0
A16	RST_N	SYSTEM RESET (ACTIVE LOW)
A17	XnD18	P4D2 P8B4 P16A12
A18	XnD19	P4D3 P8B5 P16A13

PCIE B (TOP)	SIGNAL	FUNCTION
B1	NC	NOT CONNECTED
B2	NC	NOT CONNECTED
B3	<i>GND</i>	POWER SUPPLY GROUND
B4	NC	NOT CONNECTED
B5	<i>3V3</i>	POWER SUPPLY 3.3V
B6	XnD02	P4A0 P8A0 P16A0 P32A20
B7	XnD03	P4A1 P8A1 P16A1 P32A21
B8	<i>GND</i>	POWER SUPPLY GROUND
B9	XnD04	P4B0 P8A2 P16A2 P32A22
B10	XnD10	P1C0
B11	XnD05	P4B1 P8A3 P16A3 P32A23
KEY	KEY	MECHANICAL KEY
B12	XnD14	P4C0 P8B0 P16A8 P32A28
B13	XnD15	P4C1 P8B1 P16A9 P32A29
B14	<i>CLK</i>	SLICE CLOCK
B15	XnD22	P1G0
B16	<i>GND</i>	POWER SUPPLY GROUND
B17	XnD16	P4D0 P8B2 P16A10
B18	XnD17	P4D1 P8B3 P16A11

4.2 Triangle Socket (J4/J7)

PCIE A (BOT)	SIGNAL	FUNCTION and PORTS
A1	NC	NOT CONNECTED
A2	5V	POWER SUPPLY 5V
A3	X0D12	P1E0
A4	X0D23	P1H0
A5	GND	POWER SUPPLY GROUND
A6	X0D32	P4E2 P8C6 P16B6
A7	X0D33	P4E3 P8C7 P16B7
A8	X0D25	P1J0
A9	X0D30	P4F2 P8C4 P16B4
A10	GND	POWER SUPPLY GROUND
A11	X0D31	P4F3 P8C5 P16B5
KEY	KEY	MECHANICAL KEY
A12	X0D42	P8D6 P16B14
A13	X0D43	P8D7 P16B15
A14	GND	POWER SUPPLY GROUND
A15	X0D35	P1L0
A16	RST_N	SYSTEM RESET (ACTIVE LOW)
A17	X0D40	P8D4 P16B12
A18	X0D41	P8D5 P16B13

PCIE B (TOP)	SIGNAL	FUNCTION
B1	NC	NOT CONNECTED
B2	X0D00	P1A0
B3	<i>GND</i>	POWER SUPPLY GROUND
B4	X0D11	P1D0
B5	<i>3V3</i>	POWER SUPPLY 3.3V
B6	X0D26	P4E0 P8C0 P16B0
B7	X0D27	P4E1 P8C1 P16B1
B8	<i>GND</i>	POWER SUPPLY GROUND
B9	X0D28	P4F0 P8C2 P16B2
B10	X0D34	P1K0
B11	X0D29	P4F1 P8C3 P16B3
KEY	KEY	MECHANICAL KEY
B12	X0D36	P1M0 P8D0 P16B8
B13	X0D37	P1N0 P8D1 P16B9
B14	<i>CLK</i>	MAIN SYSTEM CLOCK
B15	X0D24	P1I0
B16	<i>GND</i>	POWER SUPPLY GROUND
B17	X0D38	P1O0 P8D2 P16B10
B18	X0D39	P1P0 P8D3 P16B11

5 DEBUG/xLINK CONNECTORS (J5/J8)

The sliceKIT board has a male and female connector at each end that allows developers to connect multiple boards together to create a multiple xCORE device system connected by high speed XMOS Links between the boards.

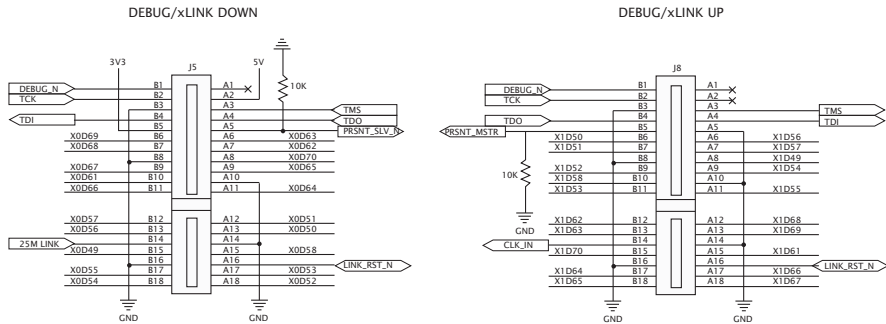


Figure 3:
xCORE-200
Debug/xLINK
DOWN/UP

The bottom of the chain can be connected via the XLINK/DBG UP to an xTAG using the xTAG adapter provided, allowing the whole system to be debugged.

5.1 DEBUG/xLINK UP (J8)

The pins on the Debug Up socket are connected to the bottom pins (X1D49-X1D70) on the 32bit port on Tile 1, as shown in the following tables, providing two 5-wire XMOS Links for each connector.

PCIE A (BOT)	SIGNAL	FUNCTION and PORTS
A1	NC	NOT CONNECTED
A2	NC	NOT CONNECTED
A3	TMS	
A4	TDI	
A5	<i>GND</i>	POWER SUPPLY GROUND
A6	X1D56	P32A7 LINK1_TX2
A7	X1D57	P32A8 LINK1_TX3
A8	X1D49	P32A0 LINK1_RX4
A9	X1D54	P32A5 LINK1_TX0
A10	<i>GND</i>	POWER SUPPLY GROUND
A11	X1D55	P32A6 LINK1_TX1
KEY	KEY	MECHANICAL KEY
A12	X1D68	P32A17 LINK2_TX2
A13	X1D69	P32A18 LINK2_TX3
A14	<i>GND</i>	POWER SUPPLY GROUND
A15	X1D61	P32A10 LINK2_RX4
A16	<i>RST_N</i>	LINK RESET (ACTIVE LOW)
A17	X1D66	P32A15 LINK2_TX0
A18	X1D67	P32A16 LINK2_TX1

PCIE B (TOP)	SIGNAL	FUNCTION and PORTS	
B1	DEBUG	NOT CONNECTED	
B2	TCK		
B3	GND	POWER SUPPLY GROUND	
B4	TDO		
B5	PRSENT	POWER SUPPLY 3.3V	
B6	X1D50	P32A1	LINK1_RX3
B7	X1D51	P32A2	LINK1_RX2
B8	GND	POWER SUPPLY GROUND	
B9	X1D52	P32A3	LINK1_RX1
B10	X1D58	P32A9	LINK1_TX4
B11	X1D53	P32A4	LINK1_RX0
KEY	KEY	MECHANICAL KEY	
B12	X1D62	P32A11	LINK2_RX3
B13	X1D63	P32A12	LINK2_RX3
B14	CLK	SLICE CLOCK	
B15	X1D70	P32A19	LINK2_TX4
B16	GND	POWER SUPPLY GROUND	
B17	X1D64	P32A13	LINK2_RX1
B18	X1D65	P32A14	LINK2_RX0

5.2 DEBUG/xLINK DOWN (J5)

The pins on the Debug Down socket are connected to the bottom pins (X0D49-X0D70) on the 32bit port on Tile 0, as shown in the following tables, providing two 5-wire XMOS Links for each connector.

PCIE A (BOT)	SIGNAL	FUNCTION and PORTS	
A1	NC	NOT CONNECTED	
A2	5V	POWER SUPPLY 5V	
A3	TMS		
A4	TDO		
A5	PRSNT	POWER SUPPLY GROUND	
A6	X0D63	P32A12	LINK2_RX2
A7	X0D62	P32A11	LINK2_RX3
A8	X0D70	P32A19	LINK2_TX4
A9	X0D65	P32A14	LINK2_RX0
A10	GND	POWER SUPPLY GROUND	
A11	X0D64	P32A13	LINK2_RX1
KEY	KEY	MECHANICAL KEY	
A12	X0D51	P32A2	LINK1_RX2
A13	X0D50	P32A1	LINK1_RX3
A14	GND	POWER SUPPLY GROUND	
A15	X0D58	P32A9	LINK1_TX4
A16	RST_N	LINK RESET (ACTIVE LOW)	
A17	X0D53	P32A4	LINK1_RX0
A18	X0D52	P32A3	LINK1_RX1

PCIE B (TOP)	SIGNAL	FUNCTION and PORTS
B1	DEBUG	DEBUG
B2	TCK	
B3	GND	POWER SUPPLY GROUND
B4	TDI	
B5	3V3	POWER SUPPLY 3.3V
B6	X0D69	P32A18 LINK2_TX3
B7	X0D68	P32A17 LINK2_TX2
B8	GND	POWER SUPPLY GROUND
B9	X0D67	P32A16 LINK2_TX1
B10	X0D61	P32A10 LINK2_RX4
B11	X0D66	P32A15 LINK2_TX0
KEY	KEY	MECHANICAL KEY
B12	X0D57	P32A8 LINK1_TX3
B13	X0D56	P32A7 LINK1_TX2
B14	CLK	MAIN SYSTEM CLOCK
B15	X0D49	P32A0 LINK1_RX4
B16	GND	POWER SUPPLY GROUND
B17	X0D55	P32A6 LINK1_TX1
B18	X0D54	P32A5 LINK1_TX0

6 xSYS Adapter

A standard XMOS xSYS interface is provided with the kit to allow host debug of the board via JTAG.

An XTAG debug adapter can be plugged into the JTAG connector using the xSYS adapter provided to allow running/debugging code, programming the FLASH memory and selection of boot mode. The xSYS adapter includes a 20-way IDC header that is used as the physical connector and the pinout of this is shown below:

XSYS signal	xCORE GPIO	Header pin	Description
TMS	See note	7	JTAG Test Mode Select.
TCK	See note	9	JTAG Test Clock.
TDI	See note	5	JTAG Test Data In. From debug adapter to XE216.
TDO	See note	13	JTAG Test Data Out. From XE216 to debug adapter.
RST_N	See note	15	System Reset. Active low, resets XE216 device
GND		4, 8, 12, 16, 20	Ground.
XL_UP1	X0D55	6	XMOS link, uplink bit 1
XL_UP0	X0D54	10	XMOS link, uplink bit 0
XL_DN1	X0D52	14	XMOS link, downlink bit 1
XL_DN0	X0D53	18	XMOS link, downlink bit 0

Figure 4:
XSYS
Connector
Pinout

Notes:

- ▶ JTAG connections occupy dedicated connections

7 Boot procedure

A master core board will boot from the on-board QSPI flash (U15) and a slave core board (connected via the XLINK connector) will boot from the master core board.

The QSPI boot pins (ports P1B, P1C and P4B) are multiplexed to the flash and to the STAR slot to allow reuse as GPIO once the XE216 has booted. At boot these pins default to being connected to the flash; subsequently these can be switched to GPIO on the STAR slot by driving X1D49 (bit 0 of port P32A) high. This procedure is not necessary on slave boards as the presence of a master board connected on XLINK/DBG UP will automatically deselect the on-board flash and connect the pins to GPIO.

8 Dimensions

The xCORE-200 sliceKIT core board dimensions are 160x90mm including the edge connectors. The mounting holes are 2mm in diameter.

9 xCORE-200 sliceKIT Portmap

For details of the complete xCORE-200 portmap and package pin outs, please refer to the published xCORE-200 Port Map².

10 Board Support

A specific XN file is required by the xTIMEcomposer tools for this board. This ships as standard with version 14.3 and later of the tools. It can be installed manually for earlier 14.x releases by using xTIMEcomposer Studio and the menu option *Help* -> *Install New Hardware*, which will show "SLICEKIT-X200". Older versions of the tools pre-14.0 are not recommended.

²<http://www.xmos.com/published/xcore-200-devices-portmap>

11 xCORE-200 sliceKIT schematics

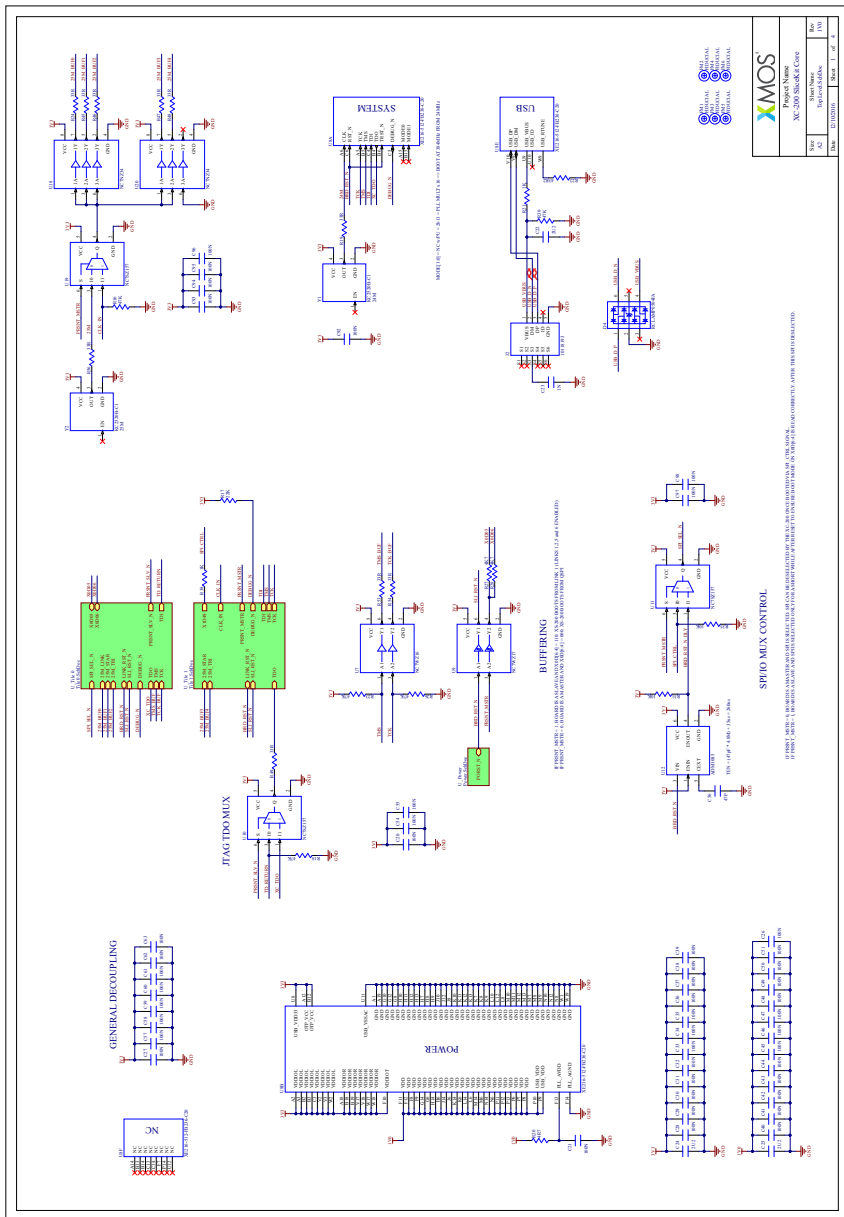
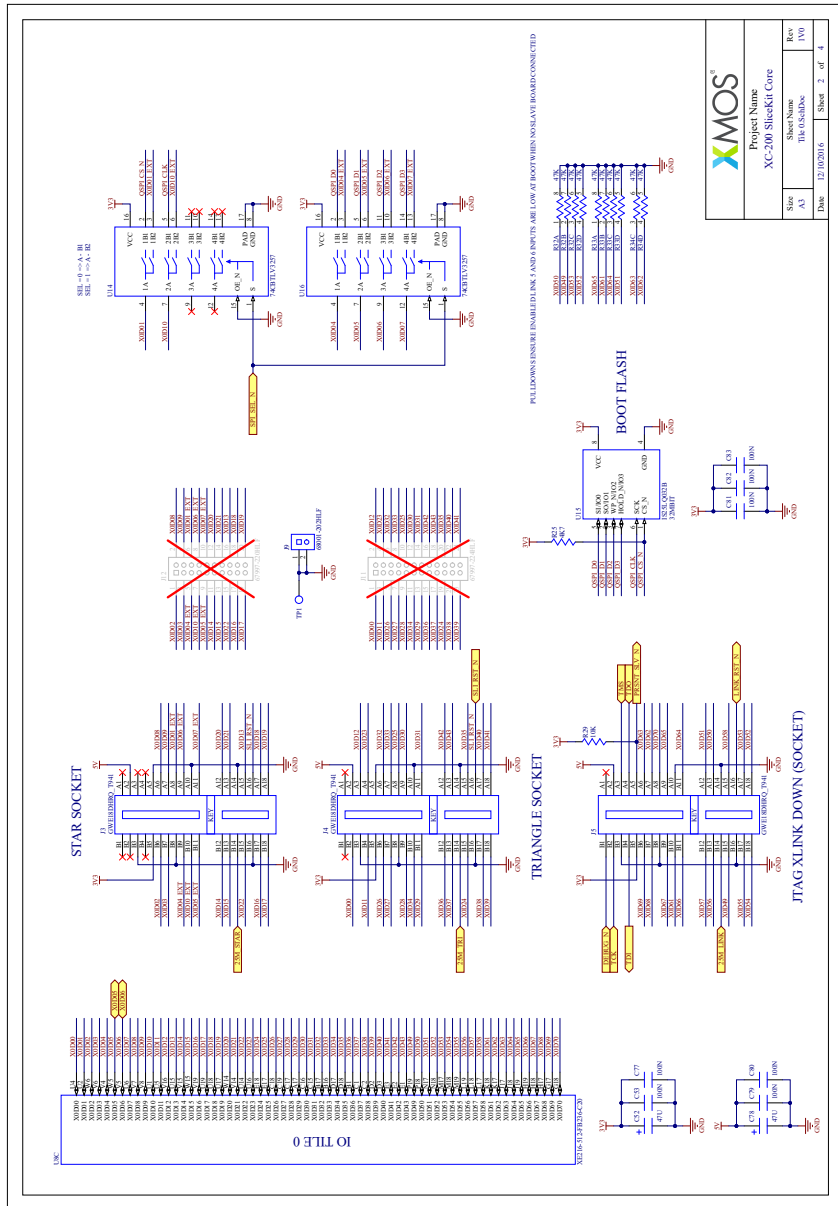


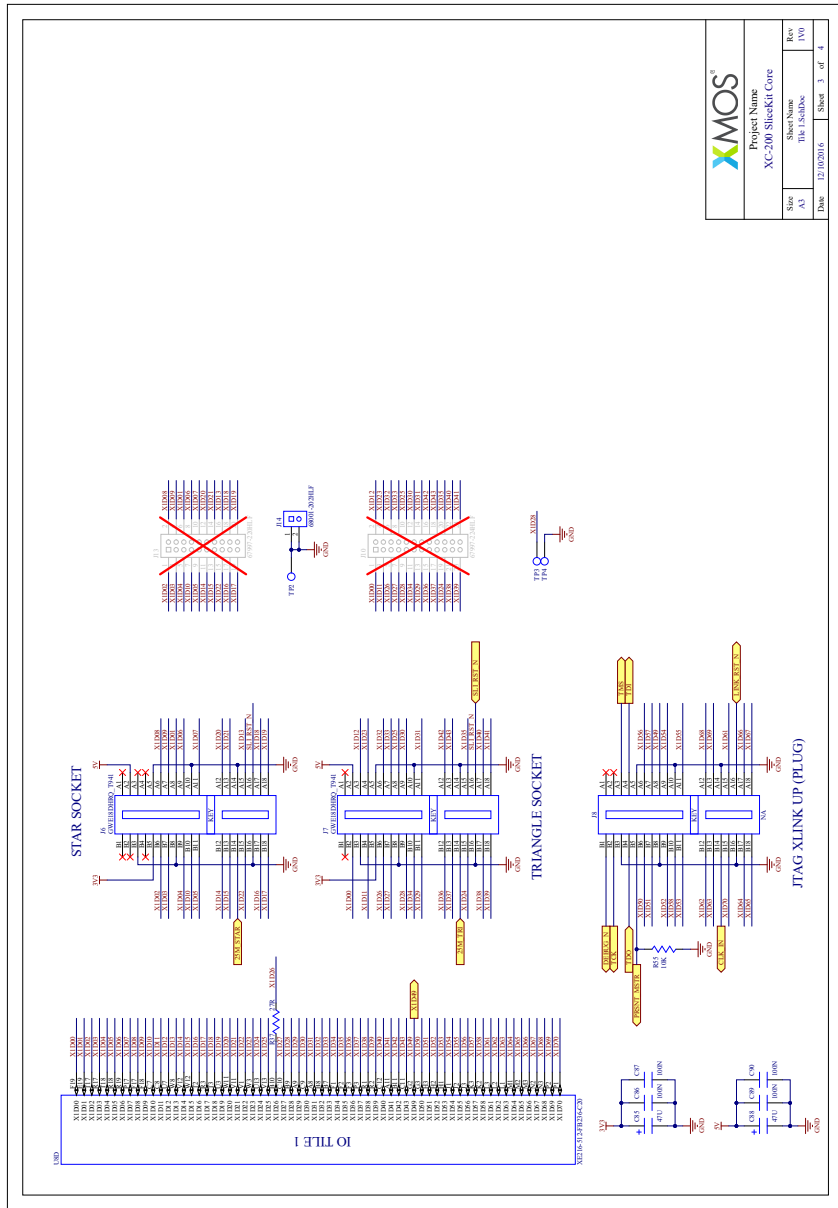
Figure 5:
xCORE-200
sliceKIT
schematic (1
of 4)



		Project Name	
		XC-200 SliceKIT Core	
Size	Sheet Name	Rev	
J15	104-000000	1	1/11
Date	12/10/2016	Sheet 2	of 4

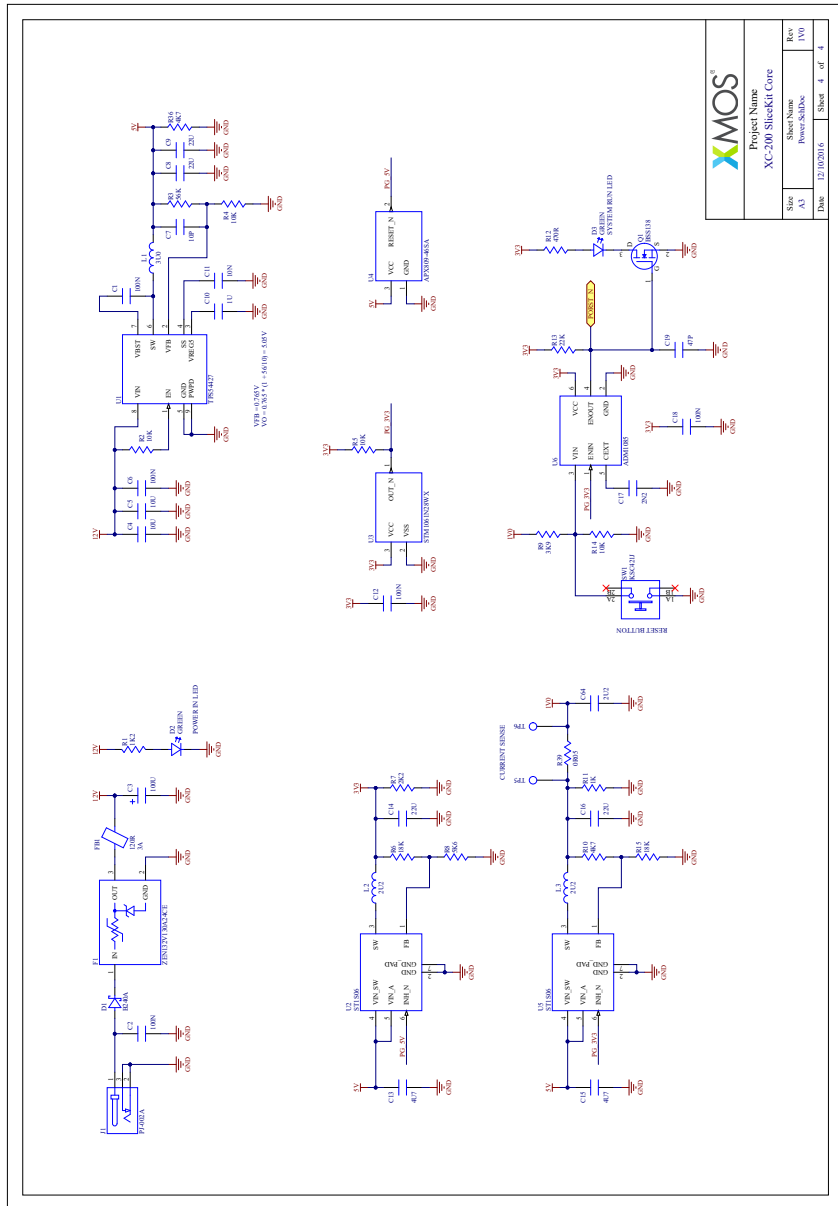
Figure 6:
xCORE-200
sliceKIT
schematic (2
of 4)

Figure 7:
xCORE-200
sliceKIT
schematic (3
of 4)



X MOS	
Project Name XC-200 SliceKIT Core	
Size A5	Sheet Name HW-1616016
Date 12/10/2016	Rev 1/1
Sheet 3 of 4	

Figure 8:
xCORE-200
sliceKIT
schematic (4
of 4)





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