Introduction

The HI5741 is a 14-bit 100MHz Digital to Analog Converter. This current out DAC is designed for low glitch and high Spurious Free Dynamic Range operation. As a result, this DAC is ideally suited for Signal Reconstruction and DDS (Direct Digital Synthesis) applications due to its inherent low noise design.

Architecture

The HI5741 DAC is designed with a split architecture to minimize glitch while maximizing linearity. Figure 1 shows the functional architecture of the device. The 10 least significant bits of the converter are derived by a traditional R/2R network to binarily weight the 1.28mA (nominal) current sources. The upper 4, or most significant bits, are implemented as segmented or thermometer decoded current sources. The thermometer decoder converts the incoming 4 bits to 15 control lines to enable the most significant current sources.

As shown in Figure 2, the thermometer decoder translates the 4 bit binary input data into a decode that enables individual current sources. For example, a binary code of 0110 on the data bits D10 through D13 will enable current sources I1, I2, I3, I4, I5, and I6. The thermometer decoding architecture ensures good differential non-linearity, which is further enhanced by the addition of laser trimming. Also, compared to a straight R/2R design, the worst case glitch is greatly reduced since creating the MSB current is the sum of current sources I1 through I8. Overall glitch is therefore reduced by a factor of 16. This also reduces the theoretical switching skew from current source to current source by using identically sized switches with identical gain, leakage, and transient responses.

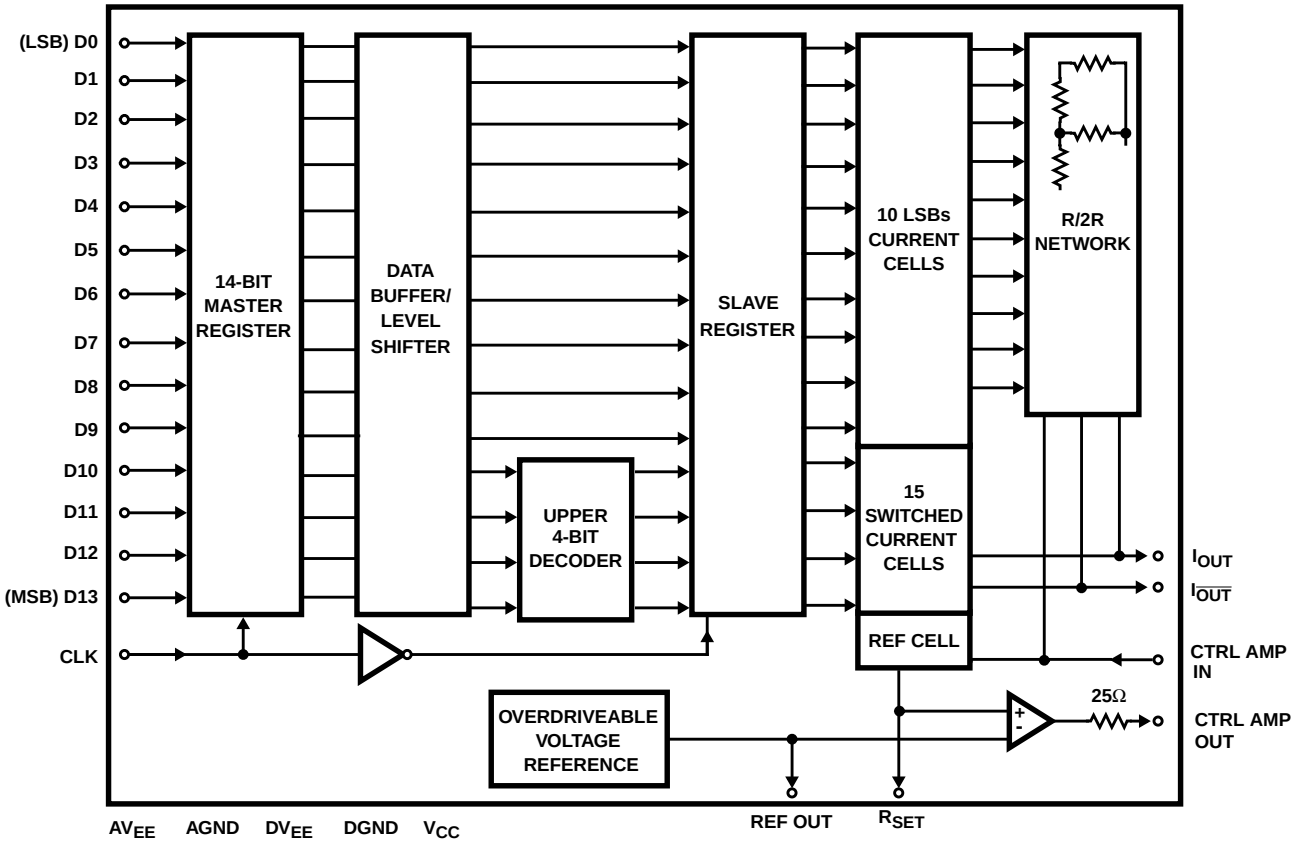

FIGURE 1. HI5741 BLOCK DIAGRAM

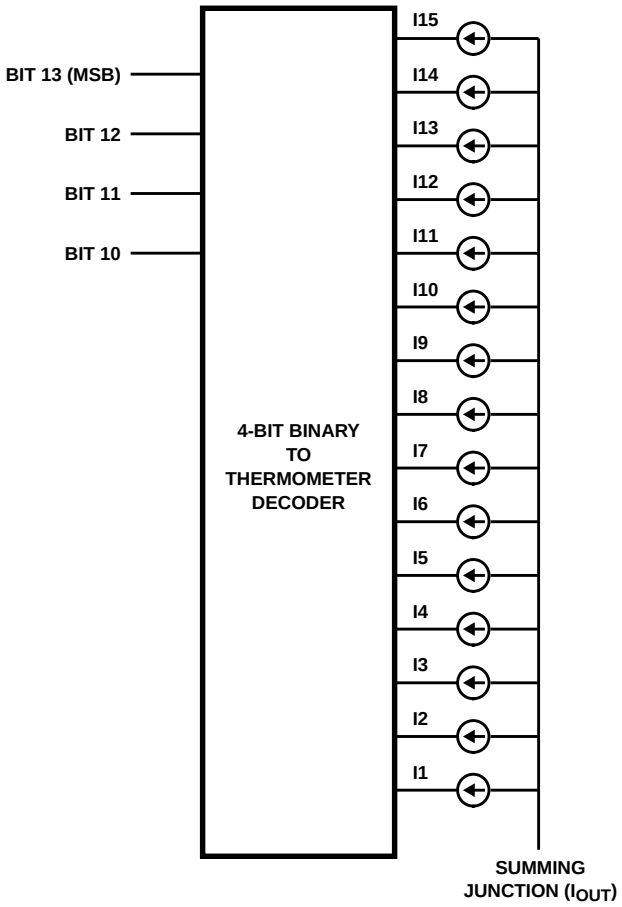

FIGURE 2. THERMOMETER DECODER

Designing to Minimize Glitch

One cause of Glitch is the time skew between bits of the incoming digital data. Typically the switching time of digital inputs are asymmetrical, meaning that the turn off time is faster than the turn on time. Unequal delay paths through the device can cause one current source to change before another. To minimize this, the Intersil HI5741 employes an internal register just prior to the current sources which is updated on the rising clock edge. In traditional DACs the worst case glitch usually occurs at the major transition i.e., 01 1111 1111 1111 to 10 0000 0000 0000. But in the HI5741 the worst case glitch is moved to the 00 0011 1111 1111 to 11 1100 000 0000 transition. This is achieved by the split R/2R segmented current source architecture. This decreases the amount of current switching at any one time and reduces the glitch by a factor of 16.

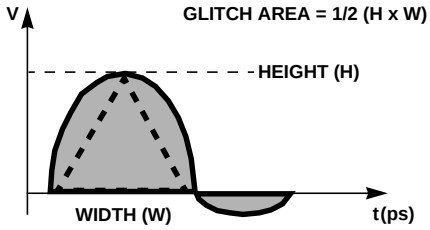

FIGURE 3. GLITCH AREA

Since the glitch is a transient event, this leads designers to believe that a simple low pass filter can be used to eliminate or reduce the size of the glitch. In effect, low pass filtering a glitch tends to “smear” the event and does little to remove the energy of the transient.

Input Timing/Logic Levels

The HI5741 has a maximum clock rate specification of 100MHz. The data setup time before the 50% point of the rising edge of the clock is t_S = 3ns (Min) and the hold time is t_H = 0.5ns (Min). Logic levels are 0.8V (Max) for an input low and 2.0V (Min) for a logic high. The HI5741 is both TTL and CMOS input compatible.

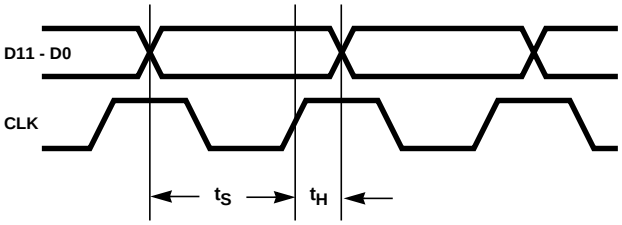

FIGURE 4. HI5741 DATA TIMING

Integral Linearity

The HI5741 has a full-scale range of 20.48mA. When driving a 64Ω load the full scale voltage swing is 0V to -1V (the internal 227Ω ladder resistance in parallel with the 64Ω load results in an equivalent 50Ω load resistance). Most video and communication applications use a $1V_{P-P}$ voltage swing which yields 20.48mA full scale current sink capability. With a $1V_{P-P}$ voltage swing on the HI5741 output an LSB is:

LSB = Full Scale Range/(2^N-1)

where N is the number of bits and the Full Scale Range is $1V_{P-P}$.

The LSB size for this application is 62.5µV. To determine the Integral Linearity of the HI5741 the bit weights of each major transition is taken. The Best Fit Straight Line method is used to calculate the overall INL. Measurements are taken at bits 0 through 9 at each bit transition. Then all combinations of the upper 4 bits are measured. Finally some worst case codes are measured and the full scale is measured. Once this is completed a best fit straight line is drawn through the data points and the worst case deviation is determined.

The worst case integral linearity of the HI5741 is specified to be less than 1.5 LSB. The implementation of laser trim assures 14-bit match from current cell to current cell. Figure 5 graphically illustrates the typical linearity performance of the HI5741.

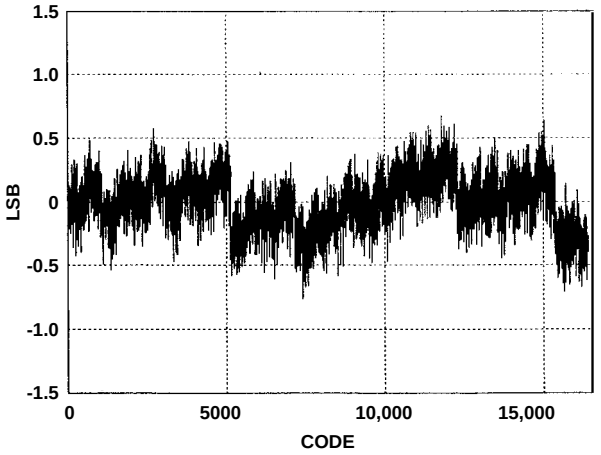

FIGURE 5A. INL TYPICAL PERFORMANCE CURVE

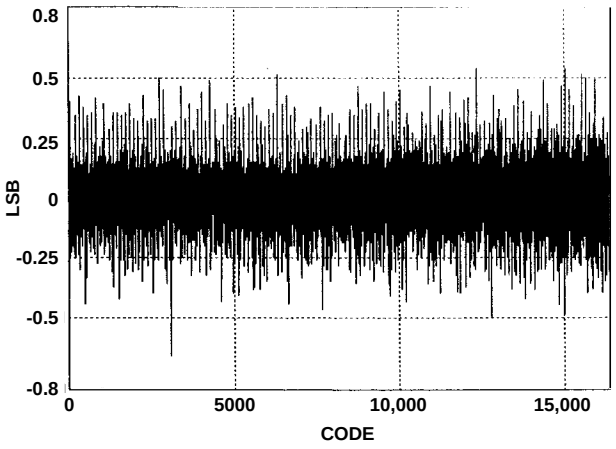

FIGURE 5B. DNL TYPICAL PERFORMANCE CURVE

Differential Linearity and Missing Codes

For a D/A Converter, the differential non-linearity is the worst case deviation from the ideal step size throughout the entire transfer curve. For the HI5741, this worst case deviation is said to be at most 1.0 LSB in magnitude. For any given D/A converter o guarantee no missing codes the converter must be monotonic.

The definition of monotonicity is; as the input code is increased the output should increase. When an input code is increased and the output of the DAC does not increase or reverses direction, then this converter is assumed to be non-monotonic, or missing codes.

Monotonicity is guaranteed as long as a DNL value of greater than -1.0 LSB is maintained.

Shown in Figure 6, as the input code increases the output voltage should increase. When an error of -1.0 LSB or less is incurred, that bit can be assumed to be a missing code since the output did not increase but rather remained the same.

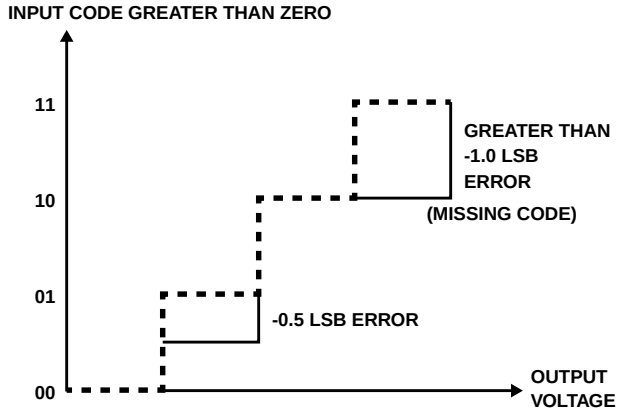

FIGURE 6. DNL EXAMPLE

The Control Amplifier

The internal control amplifier converts the reference voltage appearing on the REFOUT pin to a reference current via the circuit shown in Figure 7A. The bias voltage generated at the control amplifier output is used to mirror this current in all of the precision current cells.

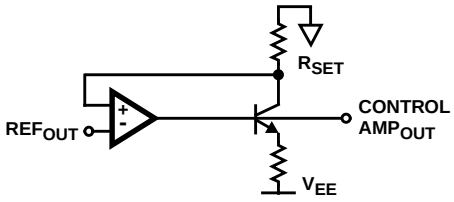

FIGURE 7A.

Adjusting Full Scale

The R_{SET} pin is used to set the Full Scale Output Current. The output current is a function of the reference voltage applied to the CONTROL AMP IN pin and the value of the R_{SET} resistor. To calculate the I_{OUT} Full Scale Current use the following formula:

I_{OUT} Full Scale = 16 x (REF_{OUT}/R_{SET})

So where REF_{OUT} = -1.20V

and R_{SET} = 931Ω

I_{OUT} = -20.62mA

To adjust the output full scale current, use a potentiometer in rheostat mode as shown in Figure 7B.

The Evaluation Board

The HI5741 Evaluation board is a 1/2 size daughter board designed to interface to the HSP-EVAL board. When used together these boards create a flexible and powerful DDS system. The HSP45116 board is used to generate the high speed digital sine wave patterns for the D/A module. The

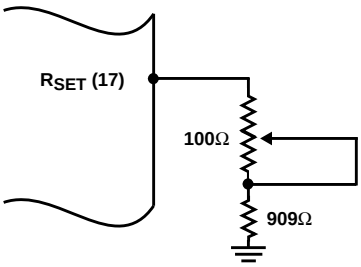

FIGURE 7B. FULL SCALE OUTPUT APPLICATION CIRCUIT

HI5741 board reconstructs the incoming digital data to an analog representation that can be analyzed on a spectrum analyzer or oscilloscope.

Plugging In

After setting-up the HSP45116 board and the HI5741 board; power should be applied to the banana jacks. A +5V, and a -5.2V supply will be needed. To reduce noise the power supply leads should be twisted pairs.

Connect the interface cable to an IBM PC or compatible's parallel port. Power should be applied to the board and then run the software directly from floppy disk. To run the software place the floppy disk into drive A: and type:

A: NCOMCTRL

the HSP45116 Control Panel will be loaded. To exercise the board the following parameters should be set:

$\overline{\text{BINFMT}}$ = 0

and then set the Center Frequency to:

CENTER FREQUENCY = 01000000_{HEX}

where the center frequency is in hex. At this point the output of the HI5741 DAC module should be converting a sine wave at 48kHz. Connect the output of the HI5741 module to an oscilloscope.

DDS Interface

The HSP45116 board is a TTL/CMOS compatible logic board. The HI5741 is a TTL/CMOS compatible logic D/A converter. The design of the DAC module is to interface to the 14 Most Significant Bits of the NCO. The HI5741 module should be plugged into P2 of the HSP-EVAL board.

Spurious Free Dynamic Range

The Spurious Free Dynamic Range of the HI5741 DAC is the most important specification for communication applications. This specification shows how Integral Linearity, Glitch, and Switching noise affect the spectral purity of the output signal. Several important things must be noted first.

When a quantized signal is reconstructed, certain artifacts are created. Let's take the example of trying to recreate a 1MHz sine wave with a $1V_{P-P}$ output. In the frequency domain the fundamental should appear at 1MHz as shown in Figure 8.

The fundamental of a pure 1MHz tone should appear as an impulse in the frequency domain at 1MHz. In a sampled system noise terms are produced near the sampling frequencies called aliases. These aliases are related to the fundamental in that they are located at $\pm f_N$ around the sampling frequency as shown in Figure 9.

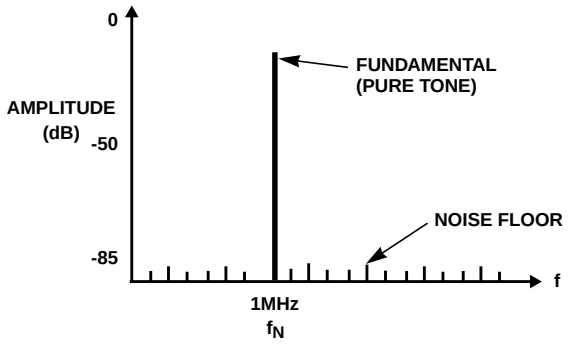

FIGURE 8. FREQUENCY PLOT OF 1MHz TONE

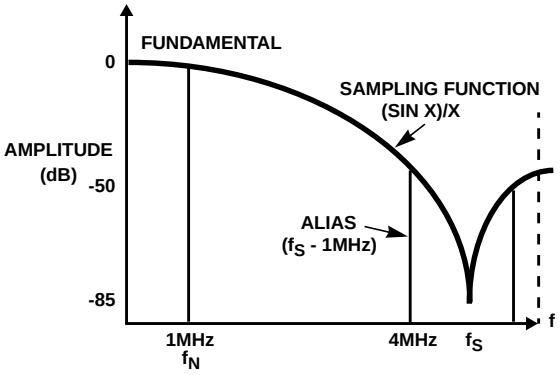

FIGURE 9. SAMPLING ALIAS PRODUCTS

So for a 1MHz fundamental and a 5MHz sampling rate an alias term is created at 4MHz and 6MHz. A (SIN)/X function shaping is also induced by sampling a signal. Aliases continue up through the frequency spectrum repeating around the sampling frequency and its harmonics (i.e., $2f_S$, $3f_S$, $4f_S$).

Also, when dealing with devices that posses high degrees of dynamic range such as the HI5741, one must contend with some fundamental limitations of the measurement system being used. Since the HI5741 typically meets (and in some cases exceeds) the dynamic range of the spectrum analyzer used to evaluate the device, the use of a notch filter can greatly alleviate the burden being placed on the equipment. By filtering out the fundamental, and in the process eliminating a large percentage of the power as seen by the spectrum analyzer, one can bring to bear the full dynamic range of the equipment, therefore truly evaluating the dynamic range of the DAC. Refer to Application Note AN9619 "Optimizing Setup Conditions for High Accuracy Measurements of the HI5741" for further details on the use of filtering for evaluation purposes.

A reconstructed sine wave out of the HI5741 is not ideal and as such has harmonics of the fundamental. The difference between the magnitude of the fundamental and the highest

noise spur whether it is harmonically related to the fundamental or not, is the definition of Spurious Free Dynamic Range. Figures 10 through 15 are sample plots taken of the HI5741 at various frequencies. In all the cases presented, the fundamental has been notched out to make maximum use of the dynamic range of the spectrum analyzer. Oscilloscope plots of the unfiltered signals are also included.

Typical Performance Curves

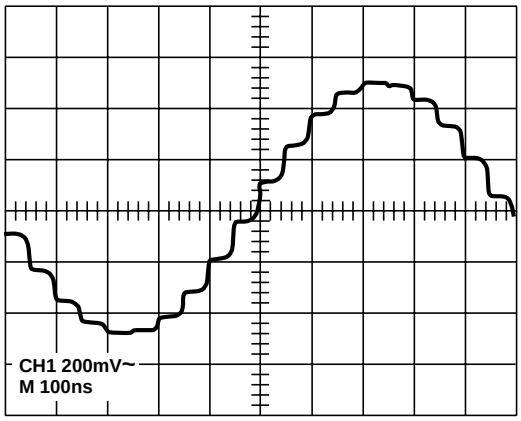

FIGURE 10A. OSCILLOSCOPE PLOT

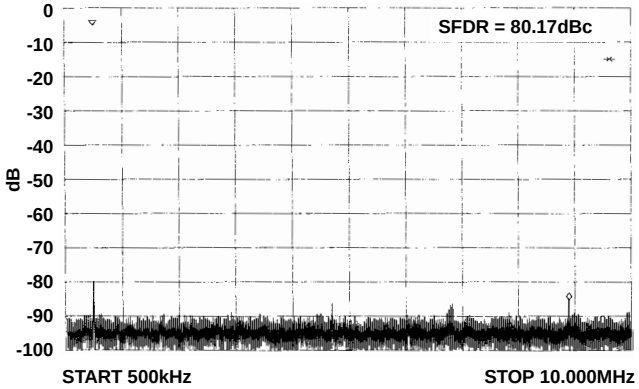

FIGURE 10B. SAMPLE PLOT

FIGURE 10. A 1MHz FUNDAMENTAL TO $\frac{f_{CLK}}{2}$. f_{CLK} = 20MHz

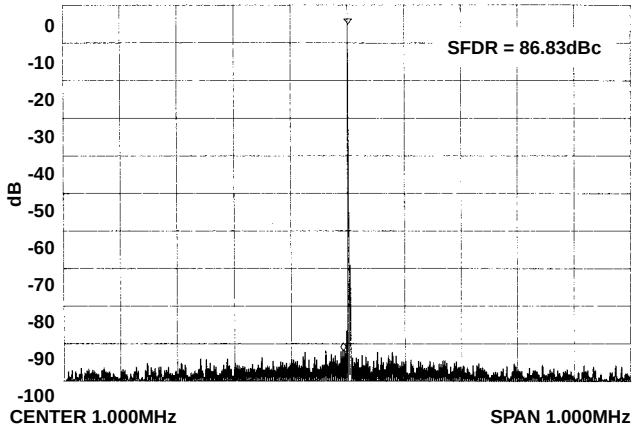

FIGURE 11. A 1MHz FUNDAMENTAL ON A 1MHz SPAN UNFILTERED

Typical Performance Curves (Continued)

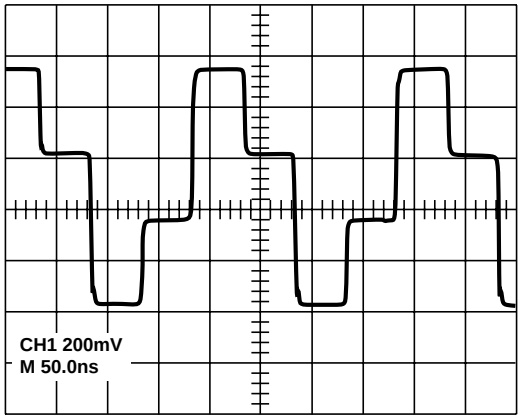

FIGURE 12A. OSCILLOSCOPE PLOT

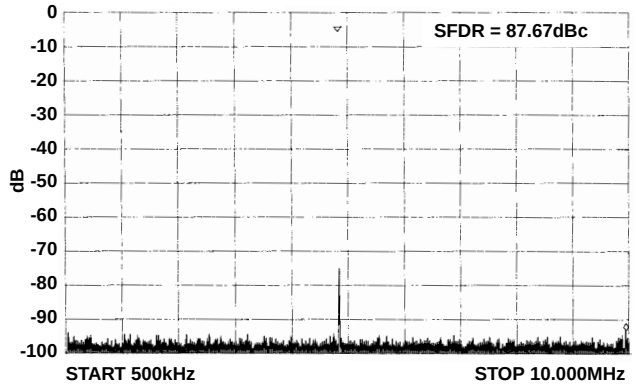

FIGURE 12B. SAMPLE PLOT

FIGURE 12. A 5MHz FUNDAMENTAL TO $\frac{f_{CLK}}{2}$. f_{CLK} = 20MHz

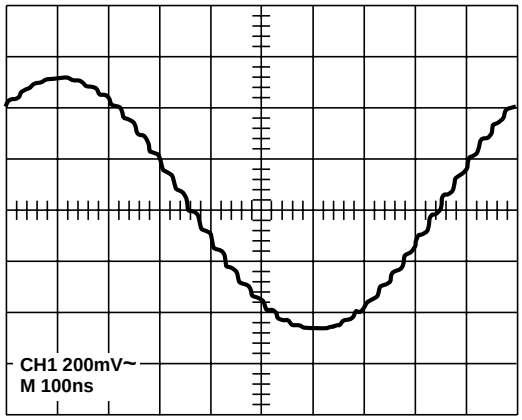

FIGURE 13A. OSCILLOSCOPE PLOT

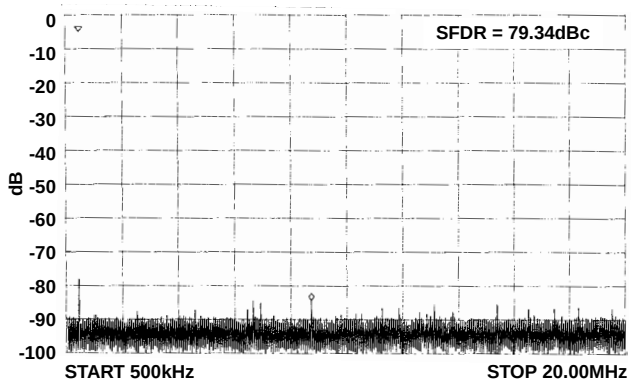

FIGURE 13B. SAMPLE PLOT

FIGURE 13. A 1MHZ FUNDAMENTAL TO $\frac{f_{CLK}}{2}$. F_{CLK} = 40MHZ

Typical Performance Curves (Continued)

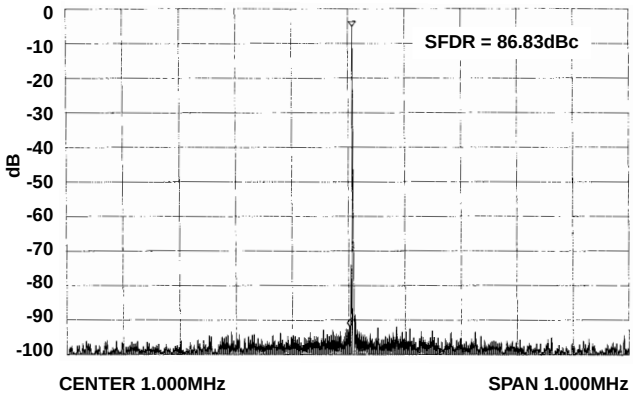

FIGURE 14. A 1MHz FUNDAMENTAL ON A 1MHz SPAN UNFILTERED

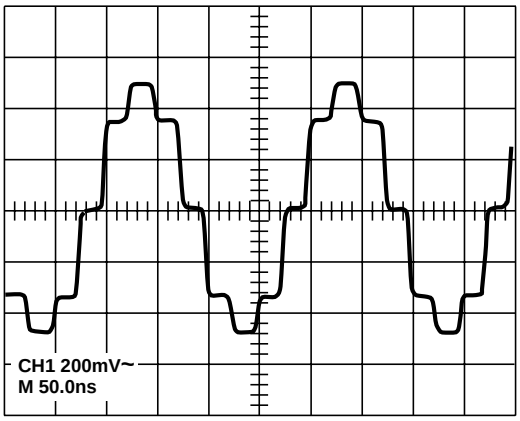

FIGURE 15A. OSCILLOSCOPE PLOT

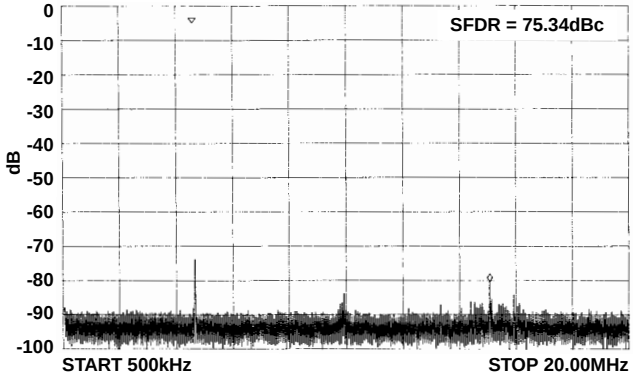

FIGURE 15B. SAMPLE PLOT

FIGURE 15. A 5MHz FUNDAMENTAL TO $\frac{f_{CLK}}{2}$. f_{CLK} = 40MHz

Using the HSP-EVAL Test Platform

The HSP-EVAL DDS platform allows quick testing of spectral properties of a given DAC. The Numerically Controlled Oscillator/Modulator (NCOM) generates digital sinewave patterns that are loaded into the DAC. The analog output of the DAC is the reconstructed sinewave pattern. The program NCOMCTRL allows downloading of the desired center frequency. The clock or sampling frequency is 25MHz. To determine the center frequency codeword the following formula is used:

$$\text{Center Frequency}_{HEX} = (\text{Desired Frequency}/25\text{MHz}) \times 2^{32}$$

This 32-bit hexadecimal word will create the fundamental. In order to ensure zero phase offset the cursor should be moved to the LOAD select. Pressing the spacebar the value should be toggled from 1 to 0 and back to 1 again. This will ensure that any previous values in the phase register are cleared and the sinewave pattern is started at zero phase.

The HSP-EVAL setup is powered from the DAC module power-supply banana jacks. The output of the setup can be observed on an oscilloscope or a spectrum analyzer.

Evaluating Multi-Tone Power Ratio (MTPR) Performance

For cellular base station users, the HI5741 evaluation module provides accessibility to the digital inputs via the edge connector. Unlike DDS applications, base station users provide multi-tone inputs to the DAC, and evaluate the dynamic range performance under these conditions.

In testing for MTPR, a ten tone pattern is created and input to the HI5741 at a clock frequency of 20MHz. One tone (typically the fifth) is removed in order to observe the third order harmonic products (2f1-f2, 2f2-f1,etc.) created by the DAC in the resulting 'dead zone'. The multi-tone power ratio of the device is then measured as the dynamic range from peak power to peak distortion.

Figures 17 and 18 graphically illustrate two examples of test patterns used to evaluate MTPR performance on the HI5741. In figure 17, a ten tone pattern is used with tones ranging from 2MHz to 3MHz with 100kHz tone spacing. Figure 18 illustrates a similar pattern, however 40kHz tone spacing is used. In both cases, the fifth tone has been removed to observe the third order harmonic products and the amount of distortion they introduce into the spectrum.

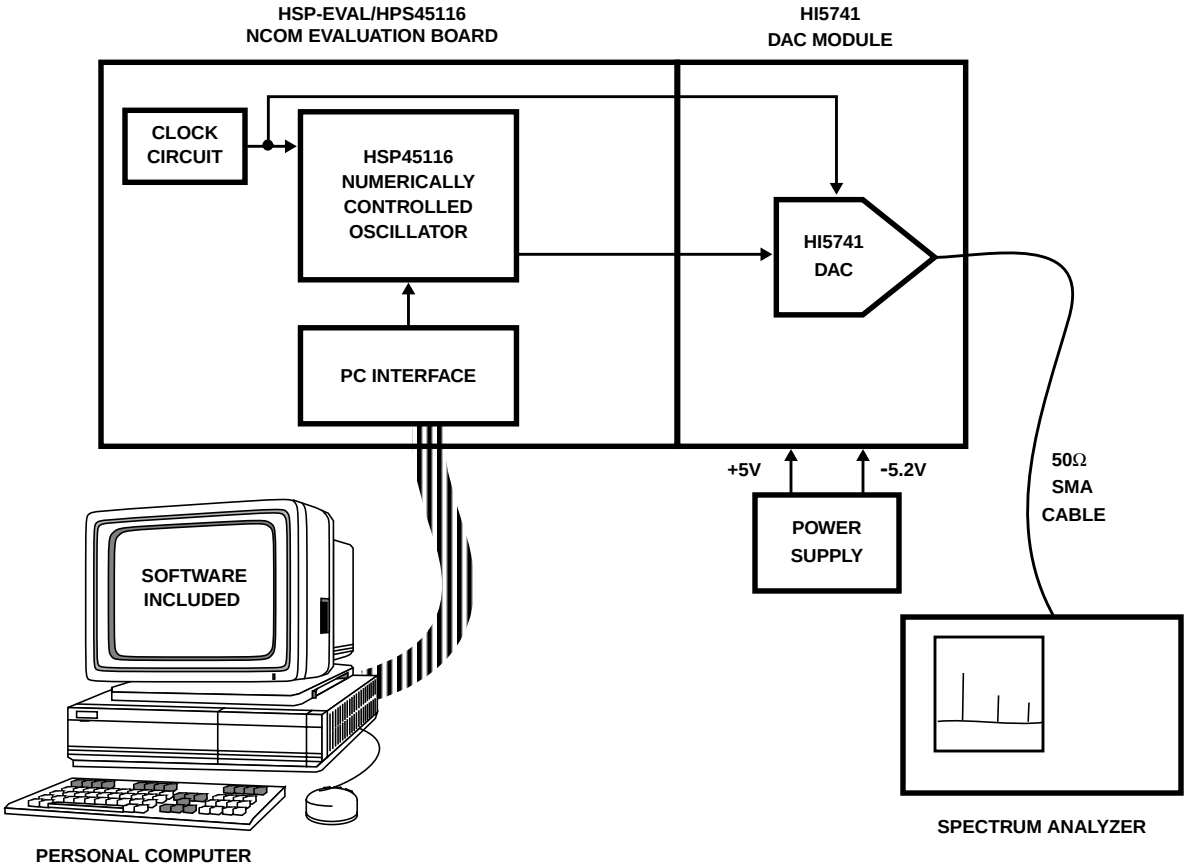

FIGURE 16. INTERSIL HI5741/DDS EVALUATION SYSTEM SETUP BLOCK DIAGRAM

Test Patterns

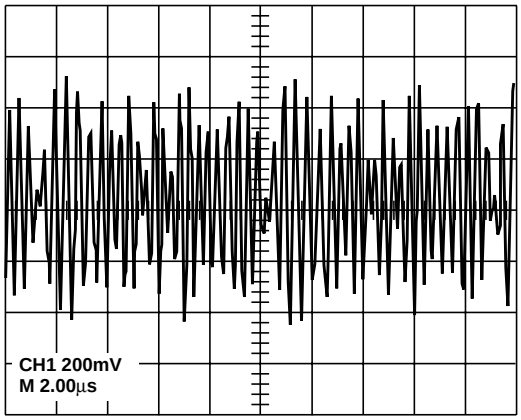

FIGURE 17A. SCOPE PLOT OF MTPR TEST WAVEFORM

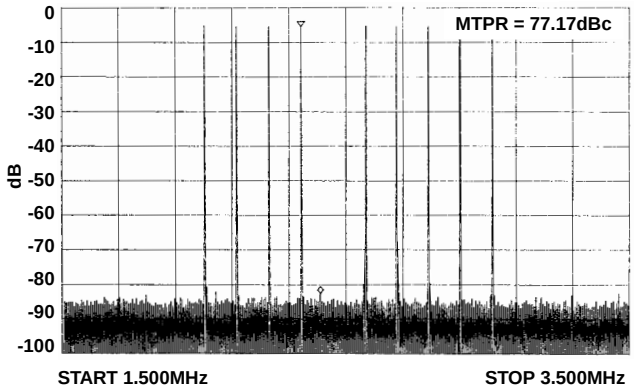

FIGURE 17B. MTPR PERFORMANCE

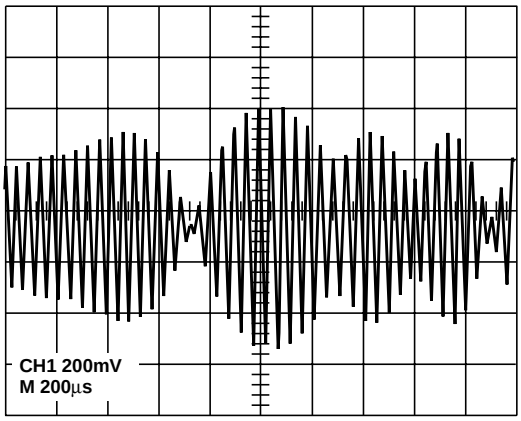

FIGURE 17C. SCOPE PLOT OF MTPR TEST WAVEFORM

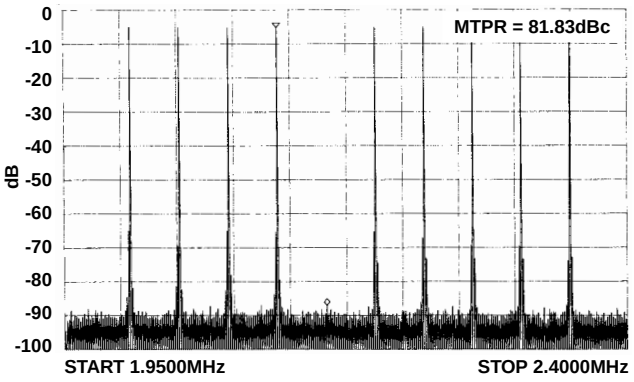

FIGURE 17D. MTPR PERFORMANCE

Schematic Diagram

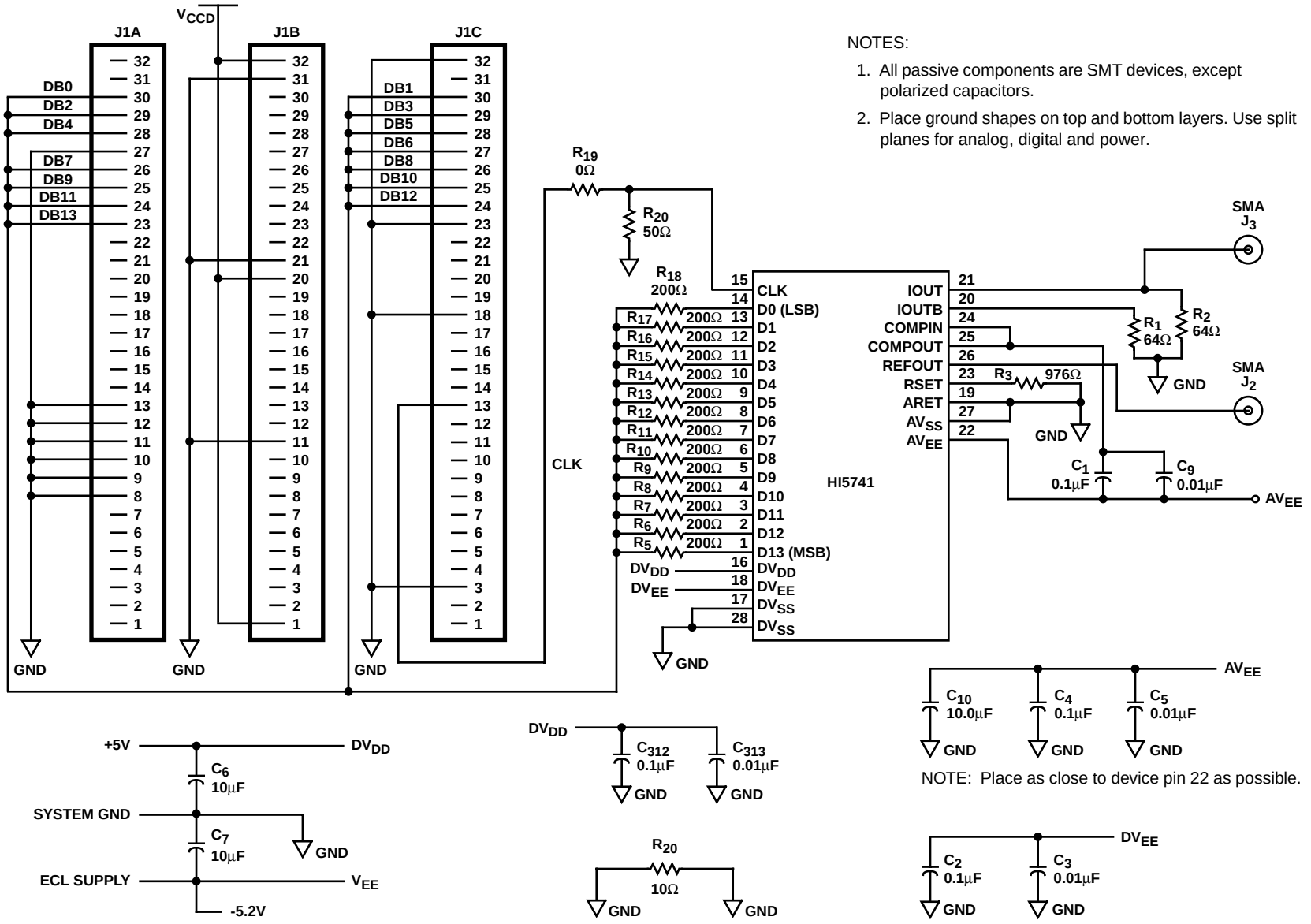

FIGURE 18.

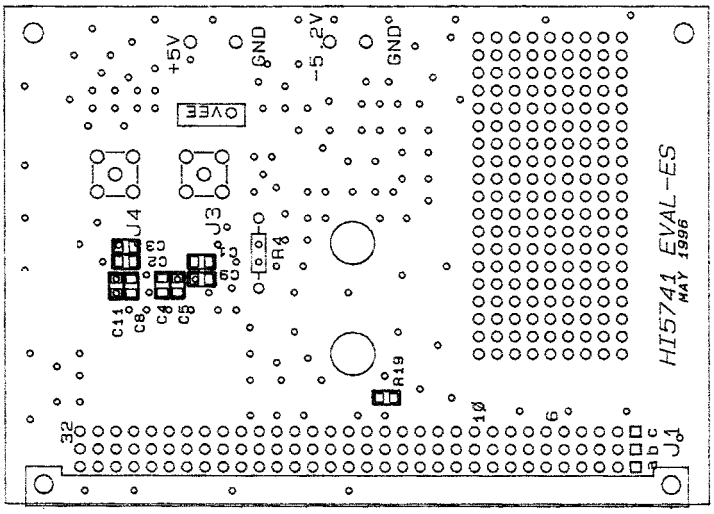

FIGURE 19A. SILKSCREEN

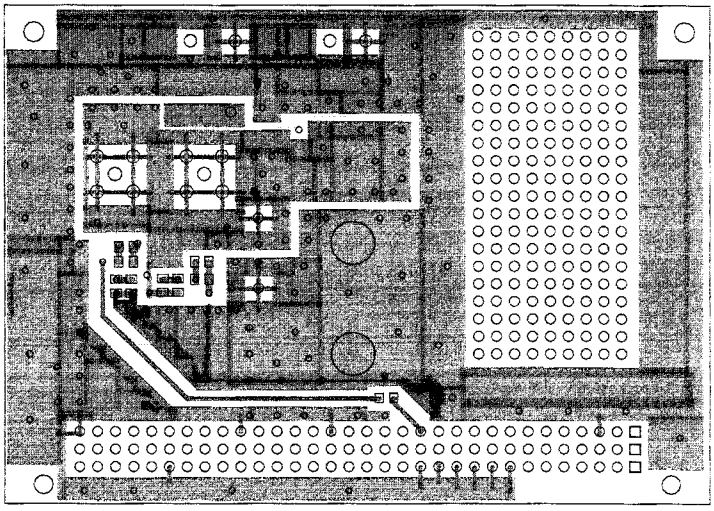

FIGURE 19B. LAYER 1

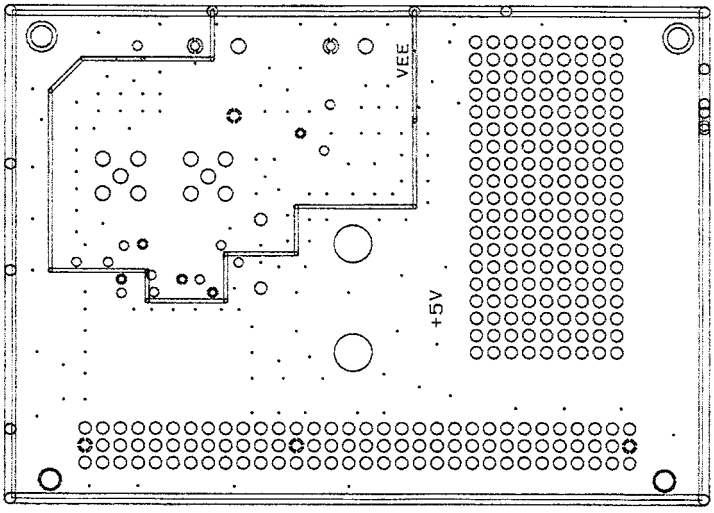

FIGURE 19C. LAYER 2

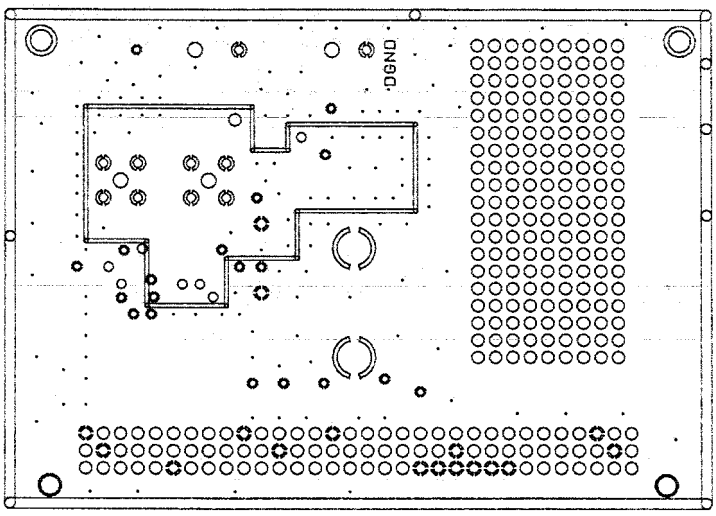

FIGURE 19D. LAYER 3

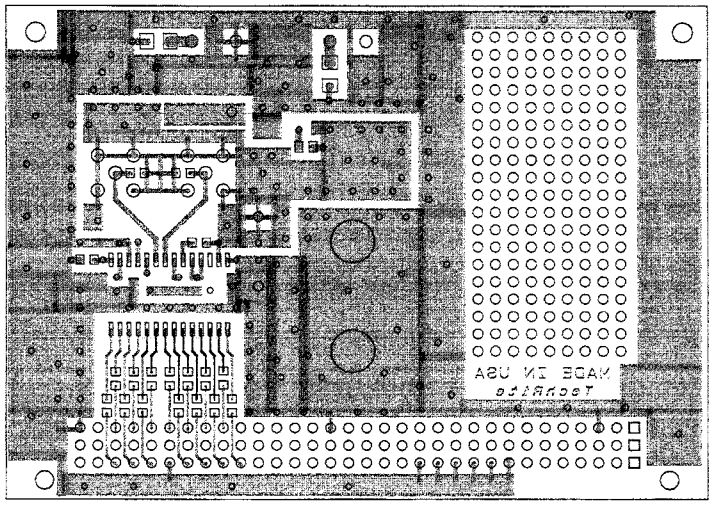

FIGURE 19E. LAYER 4

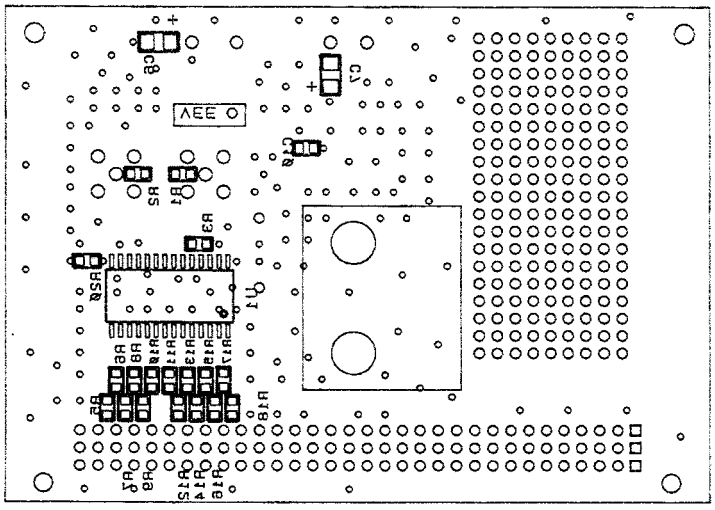

FIGURE 19F. SILKSCREEN

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