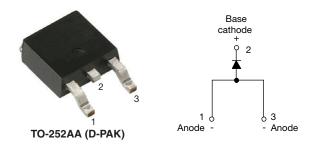
Vishay Semiconductors

High Voltage Surface Mount Input Rectifier Diode, 8 A



www.vishay.com

PRODUCT SUMMARY							
Package	TO-252AA (D-PAK)						
I _{F(AV)}	8 A						
V _R	1600 V						
V _F at I _F	1.1 V						
I _{FSM}	150 A						
T _J max.	150 °C						
Diode variation	Single die						

FEATURES

- · Glass passivated pellet chip junction
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Input rectification
- Vishay Semiconductors switches and output rectifiers which are available in identical package outlines

DESCRIPTION

The VS-8EWS16SPbF rectifier high voltage series has been optimized for very low forward voltage drop, with moderate leakage. The glass passivation technology used has reliable operation up to 150 °C junction temperature.

The high reverse voltage range available allows design of input stage primary rectification with outstanding voltage surge capability.

OUTPUT CURRENT IN TYPICAL APPLICATIONS									
APPLICATIONS	SINGLE-PHASE BRIDGE	THREE-PHASE BRIDGE	UNITS						
NEMA FR-4 or G10 glass fabric-based epoxy with 4 oz. (140 $\mu m)$ copper	1.2	1.6							
Aluminum IMS, R _{thCA} = 15 °C/W	2.5	2.8	A						
Aluminum IMS with heatsink, $R_{thCA} = 5 \text{ °C/W}$	5.5	6.5							

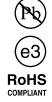
Note

• $T_A = 55 \text{ °C}, T_J = 125 \text{ °C}, \text{ footprint } 300 \text{ mm}^2$

MAJOR RATINGS AND CHARACTERISTICS									
SYMBOL	CHARACTERISTICS	VALUES	UNITS						
I _{F(AV)}	Sinusoidal waveform	8	A						
V _{RRM}		1600	V						
I _{FSM}		150	A						
V _F	8 A, T _J = 25 °C	1.10	V						
TJ		-40 to +150	°C						

VOLTAGE RATINGS			
PART NUMBER	V _{RRM} , MAXIMUM PEAK REVERSE VOLTAGE V	V _{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I _{RRM} AT 150 °C mA
VS-8EWS16SPbF	1600	1700	0.5

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VS-8EWS16SPbF Series



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ABSOLUTE MAXIMUM RATINGS									
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS					
Maximum average forward current	I _{F(AV)}	$T_C = 105 \ ^{\circ}C$, 180° conduction half sine wave	8						
Maximum peak one cycle	1	10 ms sine pulse, rated V_{RRM} applied	125	А					
non-repetitive surge current	IFSM	10 ms sine pulse, no voltage reapplied	150						
Maximum I ² t for fusing	l ² t	10 ms sine pulse, rated V _{RRM} applied	78	A ² s					
Maximum 1-t for fusing	1-1	10 ms sine pulse, no voltage reapplied	110	A-S					
Maximum I ² \sqrt{t} for fusing	l²√t	t = 0.1 ms to 10 ms, no voltage reapplied	1100	A²√s					

ELECTRICAL SPECIFICATIONS									
PARAMETER	VALUES	UNITS							
Maximum forward voltage drop	V _{FM}	8 A, T _J = 25 °C		1.1	V				
Forward slope resistance	r _t	T.I = 150 °C		20	mΩ				
Threshold voltage	V _{F(TO)}	1j = 150 C		0.82	V				
Maximum reverse leakage current		T _J = 25 °C	V _B = Rated V _{BBM}	0.05	mA				
Maximum reverse leakage current	I _{RM}	T _J = 150 °C	VR - Haled VRRM	0.50	IIIA				

THERMAL - MECHANICAL SPECIFICATIONS									
PARAMETER SYMBOL TEST CONDITIONS VALUES									
Maximum junction and storage temperature range	T _J , T _{Stg}		-40 to +150	°C					
Maximum thermal resistance, junction to case	R _{thJC}	DC operation	2.5	°C/W					
Typical thermal resistance, junction to ambient (PCB mount) ⁽¹⁾	R _{thJA}		62	0,1					
Approximate weight			1	g					
Approximate weight			0.03	oz.					
Marking device		Case style TO-252AA (D-PAK)	8EWS16S						

Note

⁽¹⁾ When mounted on 1" square (650 mm²) PCB of FR-4 or G-10 material 4 oz. (140 µm) copper 40 °C/W For recommended footprint and soldering techniques refer to application note #AN-994



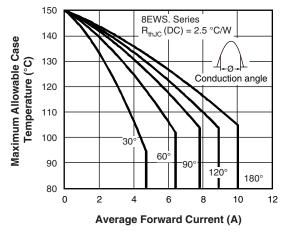


Fig. 1 - Current Rating Characteristics

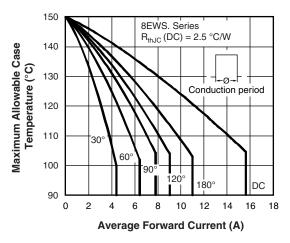


Fig. 2 - Current Rating Characteristics

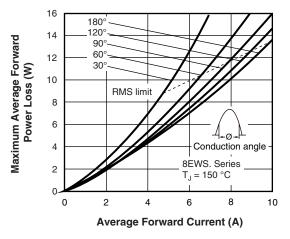
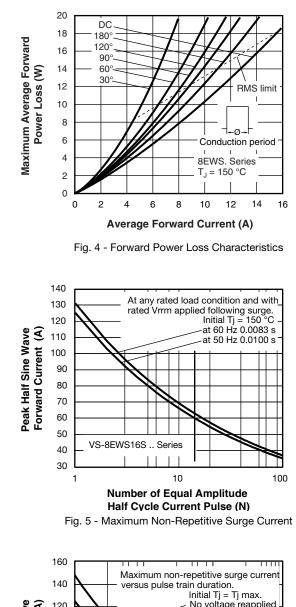


Fig. 3 - Forward Power Loss Characteristics

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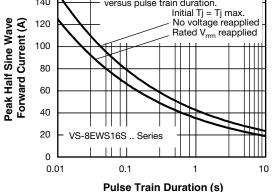


Fig. 6 - Maximum Non-Repetitive Surge Current

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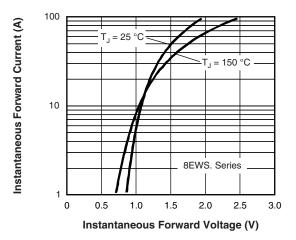


Fig. 7 - Forward Voltage Drop Characteristics

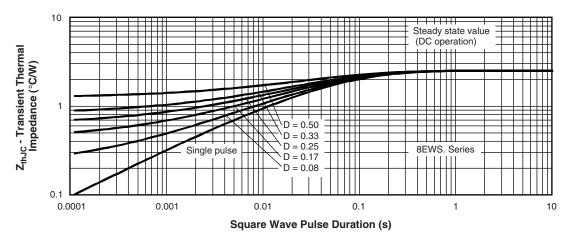


Fig. 8 - Thermal Impedance ZthJC Characteristics



ORDERING INFORMATION TABLE

evice code	VS-	8	Е	w	S	16	S	TR	Pb	
	1	2	3	4	5	6	7	8	9	
	1 -	Visł	nay Sem	iconduc	tors pro	duct				
	2 -	Cur	rent ratii	ng (8 = 8	3 A)					
	3 -	Circ	uit confi	guratior	1:					
	E = single diode									
	4 -	Pac	kage:							
		W =	D-PAK							
	5 -	Тур	e of silic	on:						
		S =	standar	d recove	ery rectif	fier				
	6 -	Volt	age rati	ng (16 =	= 1600 V	')				
	7 -	S =	surface	mounta	ble					
	8 -	• TF	R = tape	and ree	el					
		• TF	RR = tap	e and re	eel (righ	t oriente	ed)			
		• TF	RL = tap	e and re	eel (left o	oriented)			
	9 -	PbF	= lead	(Pb)-fre	е					

LINKS TO RELATED DOCUMENTS							
Dimensions	www.vishay.com/doc?95016						
Part marking information	www.vishay.com/doc?95059						
Packaging information	www.vishay.com/doc?95033						



VS-8EWS16SPbF Series

F

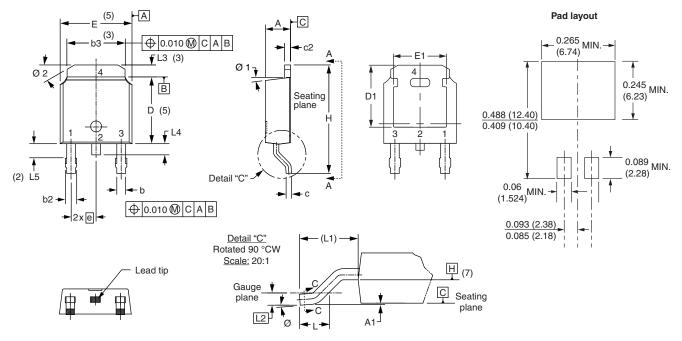
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D-PAK (TO-252AA)

DIMENSIONS in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES		IES NOTES		SYMBOL	MILLIN	IETERS	INC	HES	NOTES
STINIBUL	MIN.	MAX.	MIN.	MAX.	NOTES	NOTES	STIVIDUL	MIN.	MAX.	MIN.	MAX.	NOTES		
А	2.18	2.39	0.086	0.094			е	2.29	BSC	0.090	BSC			
A1	-	0.13	-	0.005			Н	9.40	10.41	0.370	0.410			
b	0.64	0.89	0.025	0.035			L	1.40	1.78	0.055	0.070			
b2	0.76	1.14	0.030	0.045			L1	2.74	BSC	0.108	REF.			
b3	4.95	5.46	0.195	0.215	3		L2	0.51	BSC	0.020	BSC			
с	0.46	0.61	0.018	0.024			L3	0.89	1.27	0.035	0.050	3		
c2	0.46	0.89	0.018	0.035			L4	-	1.02	-	0.040			
D	5.97	6.22	0.235	0.245	5		L5	1.14	1.52	0.045	0.060	2		
D1	5.21	-	0.205	-	3		Ø	0°	10°	0°	10°			
E	6.35	6.73	0.250	0.265	5		Ø1	0°	15°	0°	15°			
E1	4.32	-	0.170	-	3		Ø2	25°	35°	25°	35°			

Notes

⁽¹⁾ Dimensioning and tolerancing as per ASME Y14.5M-1994

⁽²⁾ Lead dimension uncontrolled in L5

⁽³⁾ Dimension D1, E1, L3 and b3 establish a minimum mounting surface for thermal pad

⁽⁴⁾ Section C - C dimension apply to the flat section of the lead between 0.13 and 0.25 mm (0.005 and 0.10") from the lead tip

(5) Dimension D, and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body

⁽⁶⁾ Dimension b1 and c1 applied to base metal only

⁽⁷⁾ Datum A and B to be determined at datum plane H

⁽⁸⁾ Outline conforms to JEDEC outline TO-252AA

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