

N-channel 80 V, 5.0 mΩ typ., 80 A STripFET™ F7 Power MOSFET in a TO-220 package

Datasheet - production data

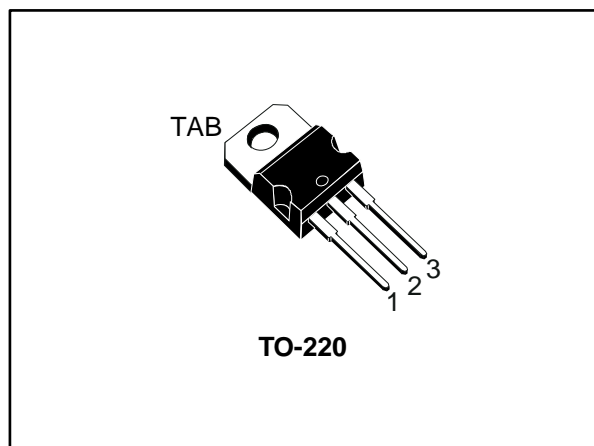
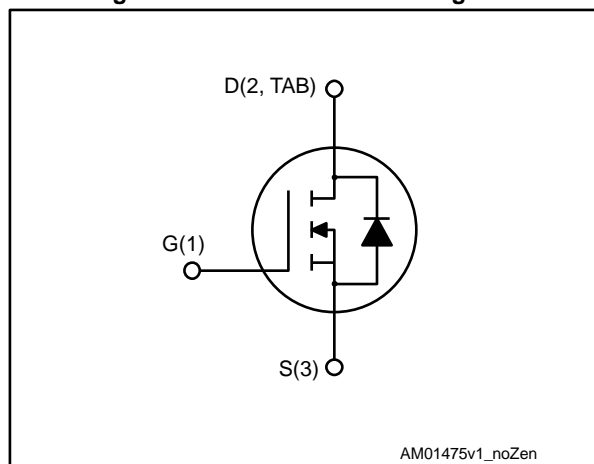


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STP130N8F7	80 V	5.8 mΩ	80 A	205 W

- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STP130N8F7	130N8F7	TO-220	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	80	A
$I_{DM}^{(1)}$	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	205	W
$E_{AS}^{(2)}$	Single pulse avalanche energy	320	mJ
T_j	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature range		

Notes:

⁽¹⁾Pulse width is limited by safe operating area

⁽²⁾Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 40\text{ A}$, $V_{DD} = 40\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.73	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	$^\circ\text{C/W}$

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 250 μA	80			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 80 V			1	μA
		V _{GS} = 0 V, V _{DS} = 80 V, T _J = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate-source leakage current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.5		4.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 40 A		5.0	5.8	mΩ

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0 V	-	4500	-	pF
C _{oss}	Output capacitance		-	1100	-	pF
C _{rss}	Reverse transfer capacitance		-	110	-	pF
Q _g	Total gate charge	V _{DD} = 40 V, I _D = 80 A, V _{GS} = 0 to 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	60	-	nC
Q _{gs}	Gate-source charge		-	25	-	nC
Q _{gd}	Gate-drain charge		-	15	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 40 V, I _D = 40 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	140	-	ns
t _r	Rise time		-	210	-	ns
t _{d(off)}	Turn-off-delay time		-	190	-	ns
t _f	Fall time		-	120	-	ns

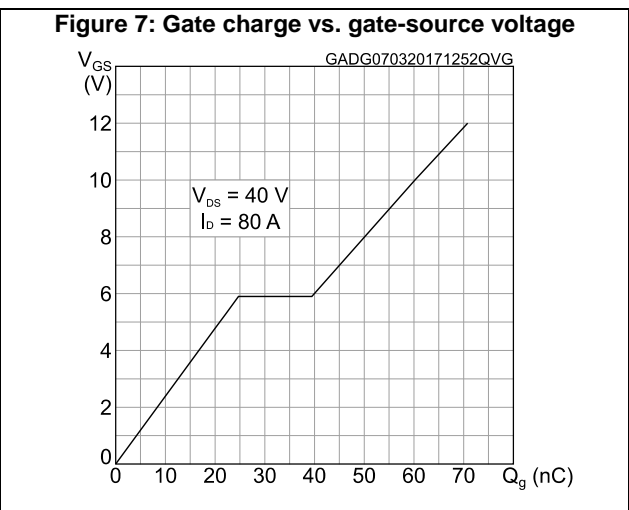
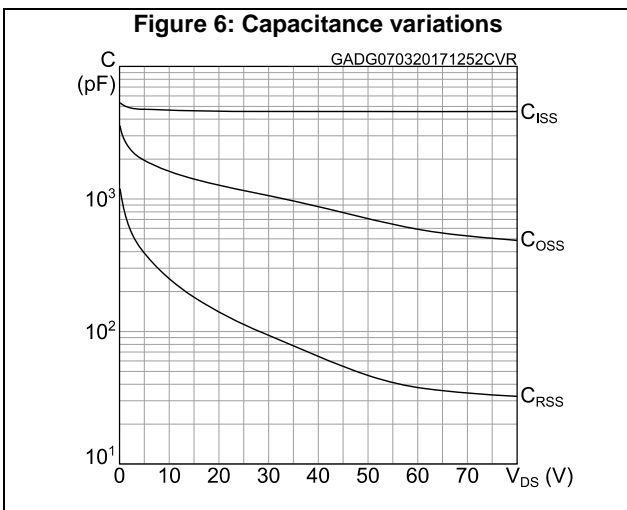
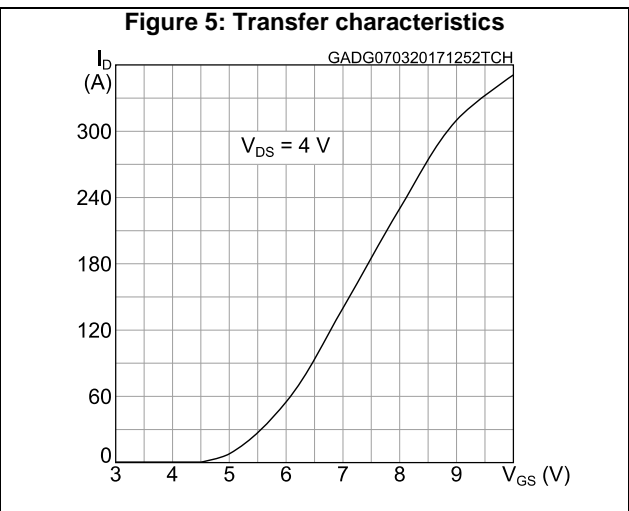
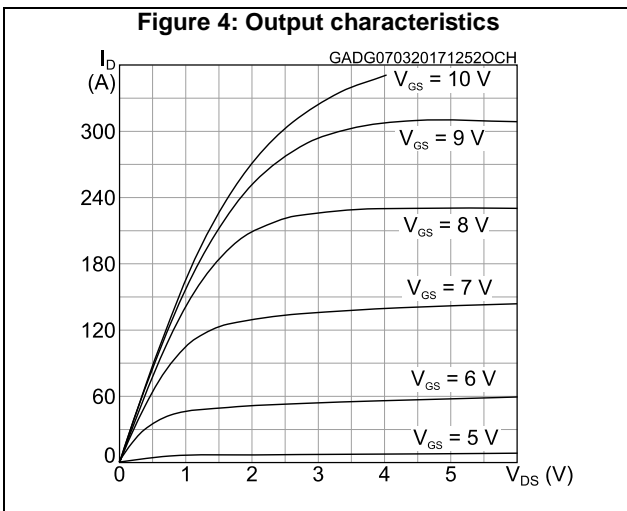
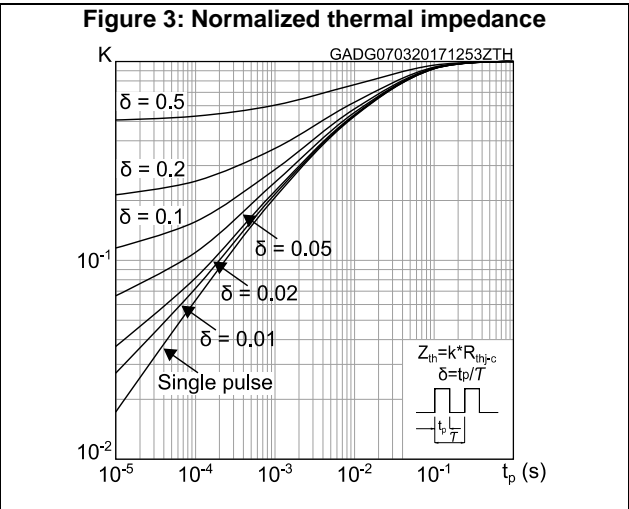
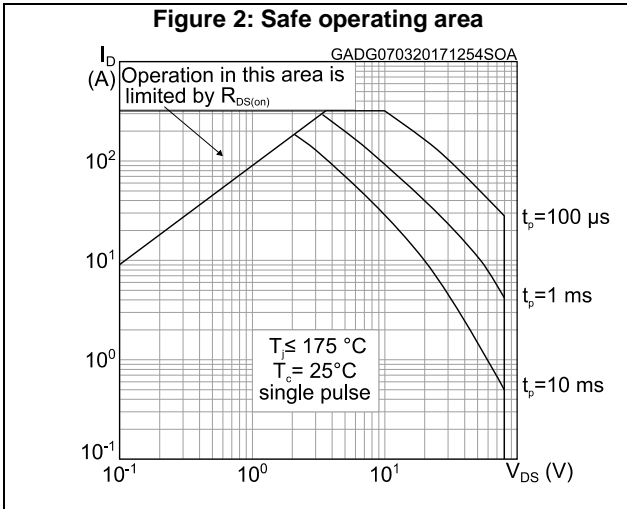
Table 7: Source drain diode

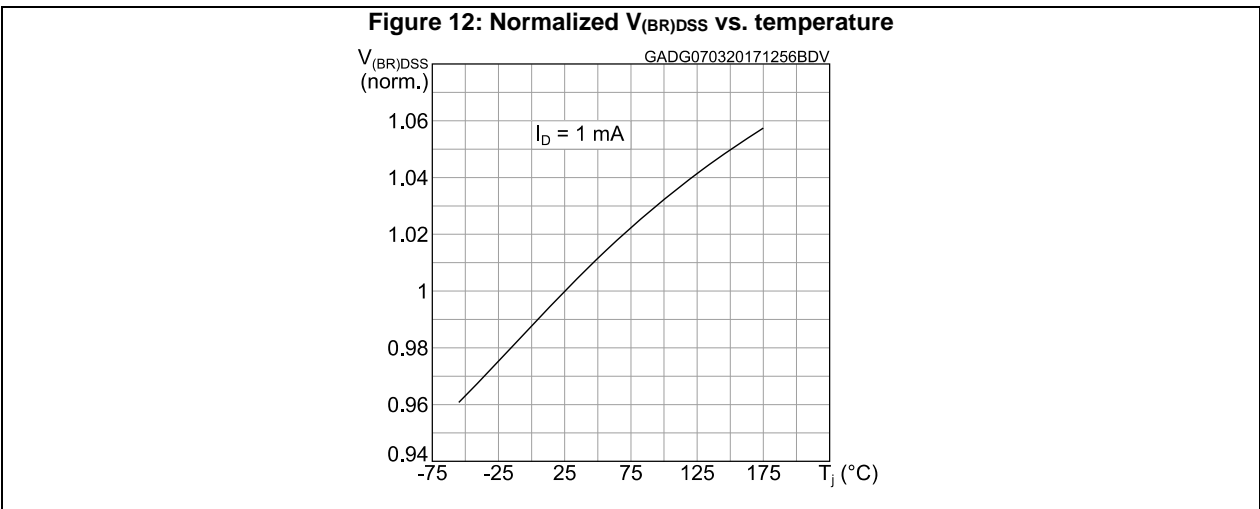
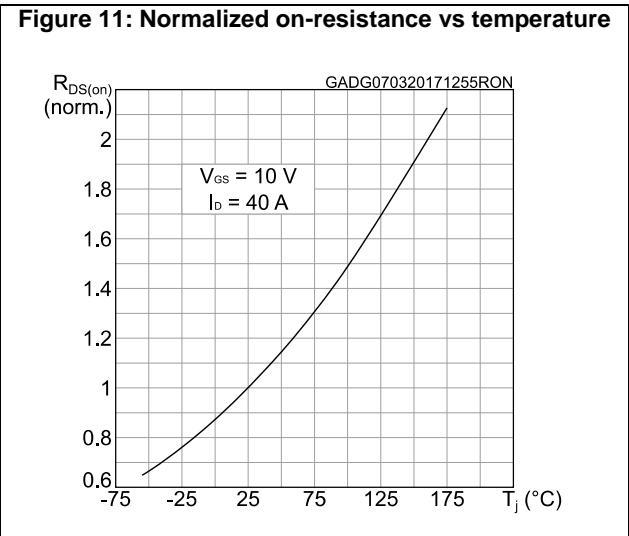
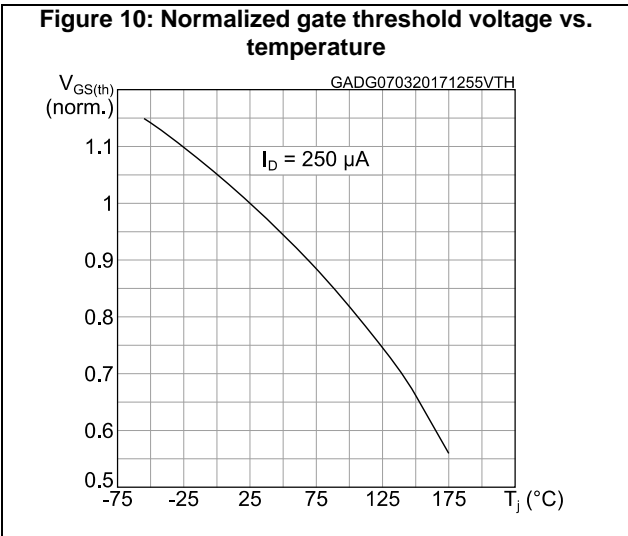
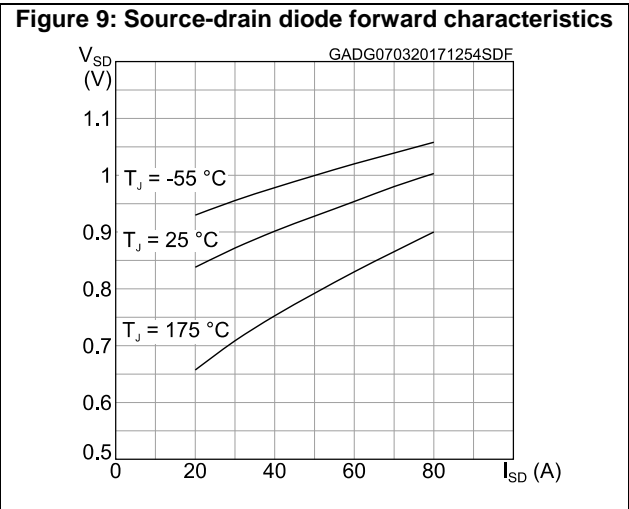
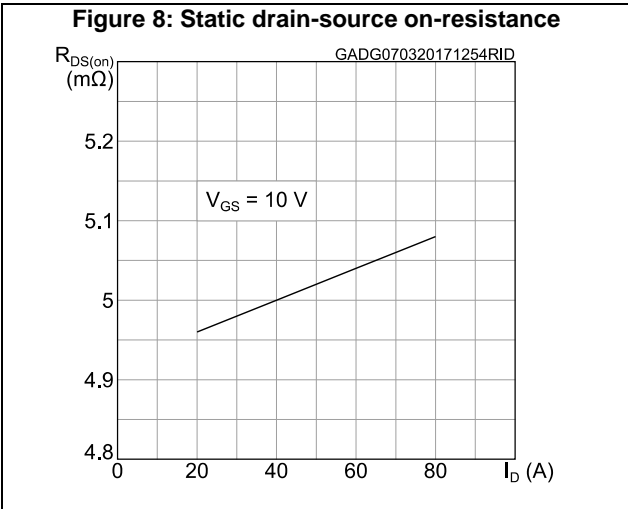
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 80 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 80 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 80 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	45		ns
Q_{rr}	Reverse recovery charge		-	54		nC
I_{RRM}	Reverse recovery current		-	2.5		A

Notes:

⁽¹⁾Pulse test: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)





3 Test circuits

Figure 13: Test circuit for resistive load switching times



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Figure 14: Test circuit for gate charge behavior



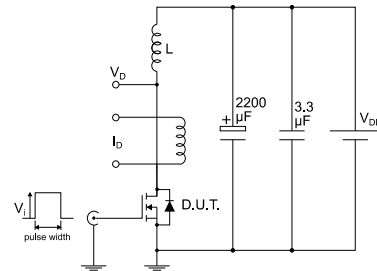
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Figure 15: Test circuit for inductive load switching and diode recovery times



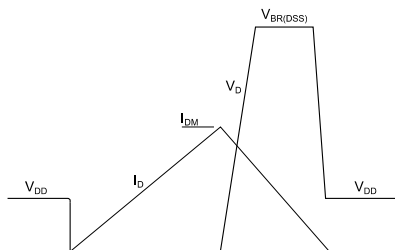
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Figure 16: Unclamped inductive load test circuit



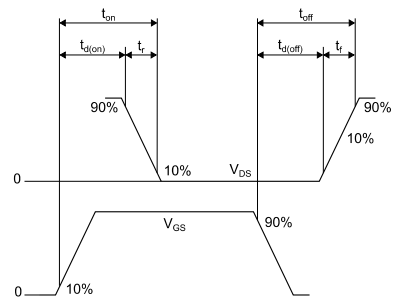
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



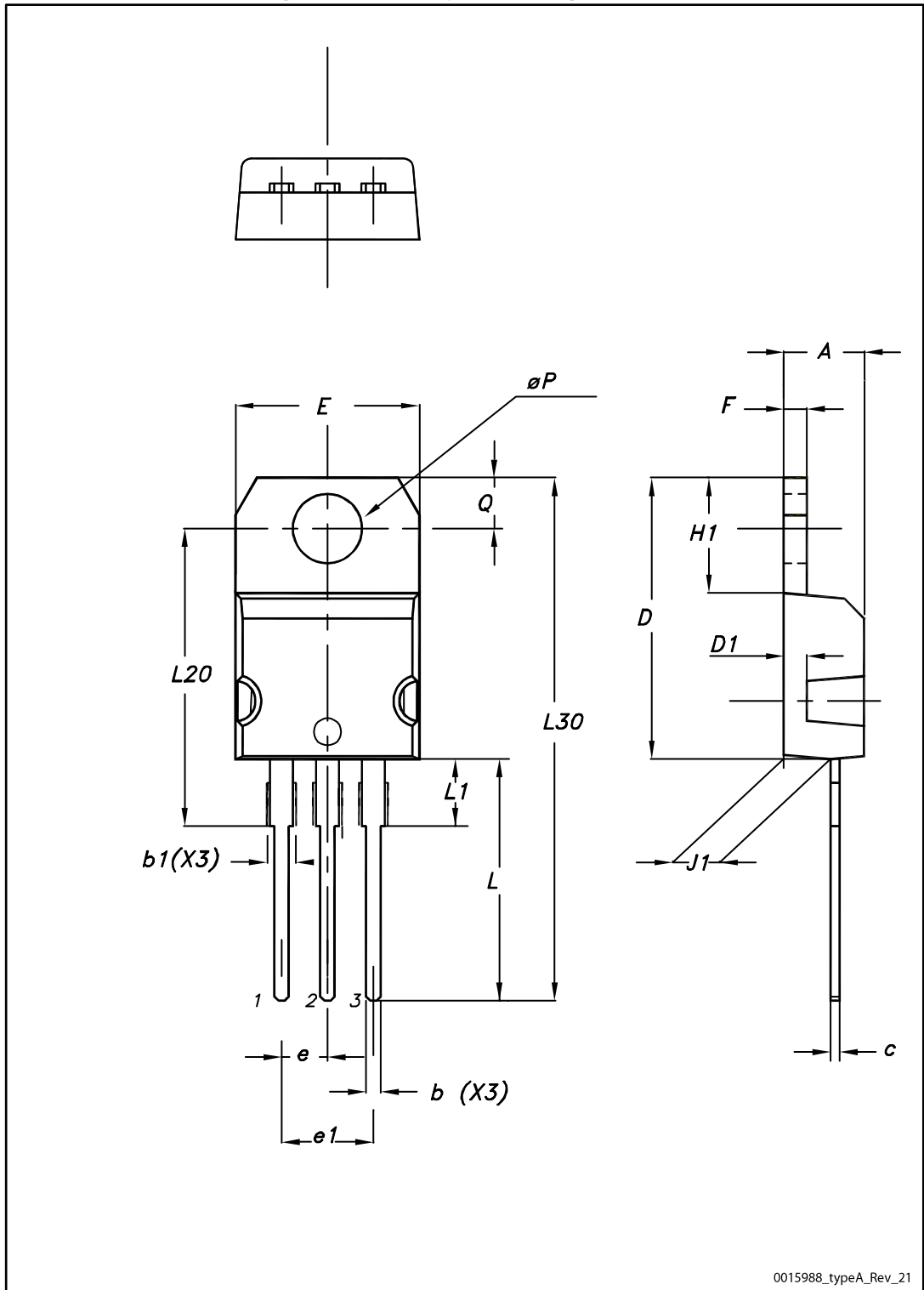
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220 package information

Figure 19: TO-220 type A package outline



0015988_typeA_Rev_21

Table 8: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
04-Dec-2014	1	First release
09-Mar-2017	2	Datasheet status promoted from preliminary to production data. Updated <i>Section 1: "Electrical ratings"</i> and <i>Section 2: "Electrical characteristics"</i> . Minor text changes

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